Guest Editorial

THE content of the International Workshop on System Level Interconnect Prediction (SLIP) pertains to the theory and application of the usable and predictable properties of optimized interconnect systems. SLIP by definition incorporates researchers from many different disciplines that range from computer system architecture to physical computer-aided design (CAD) to technology forecasting. As in the workshop, this Special Section of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS includes papers that discuss the theoretical underpinnings of interconnect prediction and the applications of these techniques to a variety of research fields.

The cornerstone of many interconnect prediction techniques is based upon a few weeks of work by an engineer at IBM in the early 1960s. He discovered that optimized digital components have input/output (I/O) attributes that follow a simple rule that bears his name—Rent's Rule. Rent's Rule has paved the way for more rigorous analyses of highly complex VLSI systems. The first paper by J. Dambre, D. Stroobandt, and J. Van Campenhout, which is entitled "Toward the accurate prediction of placement wirelength distributions in VLSI circuits," highlights the transformation of Rent's Rule to a Rent's Characteristic that was originally developed at Ghent University, Ghent, Belgium, and more accurately describes the average I/O relationships for various partitions in large logic macrocells. In fact, the authors of this paper illustrate a bi-partitioning application of the Rent's Characteristic to more accurately estimate average wire length. The authors also demonstrate a technique to rapidly extract the Rent's Characteristic from a logic netlist that is used to estimate average wire length. Ultimately, this type of rapid interconnect prediction for specific logic networks could be invaluable for an interconnect-centric VLSI design flow.

The second paper by M. R. Casu, *et al.*, which is entitled "An electromigration and thermal model of power wires for *a priori* high-level reliability prediction," is a good example of using physically based wire models along with Rentian system-level interconnect models to explore the design of power distribution networks along the International Roadmap for Semiconductors (ITRS). The authors in this paper use a physical electromigration model and Rentian wirelength distributions to estimate the minimum required physical dimensions of the wires in a power distribution network. Using the ITRS, the authors make quantitative calculations to explore power distribution designs until 2007. A salient conclusion of this analysis is that the minimum power wire width does not scale with each new technology generation due to electromigration.

Mr. Rent discovered his rule during the era of mainframe computers with large racks of printed circuit boards that used bipolar technologies; however, researchers still use his discovery to understand what is arguable the next milestone in VLSI technology—three-dimensional (3-D) integration. The third paper by S. Das, A. Chardrakasan, and R. Reif, which is entitled "Calibration of Rent's Rule models for three-dimensional integrated circuits," explores the application of Rent's Rule in three-dimensions using a physical design tool that optimizes a 3-D standard cell placement of the ISPD98 benchmark circuits. In addition, the authors develop a 3-D global router to help obtain an accurate estimation of the final wirelengths. This in-depth exploration into understanding and predicting wirelength distributions in 3-D is compared to a previous model also developed at Massachusetts Institute of Technology (MIT), Cambridge, and the authors conclude that the predicted wirelength distribution is within 20% of the final value.

The fourth paper, by J. Joyner, P. Zarkesh-Ha, and J. D. Meindl, entitled "Global interconnect design in a three-dimensional system-on-a-chip," is also focused on 3-D stacking of integrated circuits. The foundation of this paper uses a 3-D distribution developed at Georgia Institute of Technology, Atlanta, that has been rigorously derived from first principles. Using this Rentian-based distribution, the authors systematically build and optimize every wiring tier in a two-dimensional (2-D) and 3-D system. This detailed inter-dimensional comparison enables key conclusions to be drawn on the effects that 3-D technology will have on billion transistor systems. One salient conclusion of this paper is that the current 2-D integrated circuits that are severely interconnect limited could be dramatically improved with 3-D technology such that the maximum possible wire-limited clock frequency could scale with the *square* of the technology generation scaling factor. The authors project that the enormous benefits of 3-D IC stacking can be achieved if the obstacles of high I/O density and heat removal limitations in 3-D technology are solved.

Rent's discovery is not only important to technologist looking to understand the impact of new technology on future digital systems. Computer architects can also use these wire distribution predictions to understand the impact of micro-architectural choices on system clock frequency, die size, number of metal levels, and power dissipation. The next paper by S. Wadekar and A. Parker, which is entitled "Interconnect-based system-level energy and power prediction to guide architectural exploration," is a good example of using interconnect prediction to estimate power dissipation so as to guide the designer toward more efficient micro-architectures. A key attribute of this paper is an empirical switching activity model that is correlated to wire length and is used to estimate the power dissipation of each design option. Using their new technique, the authors have shown evidence that they can predict the power dissipation *before* synthesis within 10% of the post-synthesis estimated value.

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The final paper is a transactions brief by P. Kannon, S. Balachandran, and D. Bhatia entitled "On metrics for comparing interconnect estimation methods for FPGAs." This paper does a good job in presenting an overview of a variety of interconnect estimation techniques for FPGAs. Moreover, the authors propose a set of four metrics to compare these interconnect prediction techniques and draw key conclusions about the strength and weaknesses of each FPGA interconnect prediction method. They conclude that an interconnect prediction tool developed at the University of Texas at Dallas, called fGREP2 is the most accurate interconnect predictor.

I would like to thank all the authors and the reviewers for their hard work and time spent in putting this special section together. I would also like to thank the Editor-In-Chief for his guidance and support of this Special Section. For readers of this Special Section who want to find out more about this new field of system-level interconnect prediction (SLIP), please visit the SLIP workshop website at www.sliponline.org.

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He is currently an Assistant Professor in the School of Electrical and Computer Engineering at the Georgia Institute of Technology. His current research is focused on developing advanced VLSI interconnect models, optimizing multilevel interconnect networks, and applying system-level interconnect prediction to an interconnect-centric GSI design flow. He has published over 40 journal, conference, and workshop papers.

In January 2001, he was awarded the National Science Foundation CAREER Award for excellence as a young educator and researcher. In 2002, he was the General Chair for the International Workshop on System Level Interconnect Prediction, and he is currently a Guest Editor for a Special Section of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. In April 2003, he received the Outstanding Junior Faculty Award from the School of Electrical and Computer Engineering, Georgia Institute of Technology.