Guest Editorial

FOR ALL THE integrated circuits used in battery-powered portable devices, power consumption is the main issue. Furthermore, power consumption is also a main issue for high-performance integrated circuits due to heat dissipation. Consequently, power consumption is a dramatic problem for all integrated circuits designed today. This Special Section will appear in two parts for logistic reasons and presents nine regular papers and two brief papers, which have been selected mainly from the International Symposium on Low-Power Electronics and Design (ISLPED'02) Conference in Monterey, CA, August 12-14, 2002. The second part of the Special Section will appear in the next issue of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. We are grateful to all the authors and reviewers.

While the reduction of the dynamic power has been the major focus in designing low-power chips in the past, addressing static power is a vital issue in the new very deep-submicron technologies. The first four papers of this issue present techniques to reduce leakage power at the circuit, gate, and microarchitectural levels. The first paper, *Statistical Analysis of Subthreshold Leakage Current for VLSI Circuits*, by Rao *et al.* presents a method for estimating the variation of subthreshold leakage due to gate-length variability. This method is accurate and mitigates the pessimism produced by other estimation methods. The second paper, *Leakage Current Reduction in CMOS VLSI Circuits by Input Vector Control*, by Abdollahi *et al.* describes a technique for leakage reduction in standby mode by applying and propagating through additional logic low leakage input vectors to the considered logic block. The third paper, *Gate Oxide Leakage Current Analysis and Reduction for VLSI Circuits*, by Lee *et al.* addresses the growing issue of gate oxide leakage and its interaction with the subthreshold leakage. An estimation method is proposed and its accuracy is validated using many benchmark circuits in a projected 100-nm technology. In the fourth paper, *Circuit and Microarchitectural Techniques Reducing Cache Leakage Power*, Kim *et al.* presents cache architectures for which most cache lines are maintained in drowsy state, reducing the leakage power by a factor of 60%–75%.

These papers mainly address the leakage issue at the circuit and gate level and there are various opportunities to consider leakage reduction at the architecture level. It is still a research domain to decide if synthesized digital architectures, such as pipeline, parallel, asynchronous, or other architectures may be better for reducing leakage. A very low activity factor does not provide a good ratio between dynamic and static power, as an idle circuit does present the same leakage as compared to a very active circuit. To reduce the total power consumption, an attractive goal could be to have fewer, but more active transistors to perform the same logic function. If a given logic function is performed with 10 000 gates and with an activity factor of 1%, this means that on average 100 gates are switching in a clock period. If the same logic function could be implemented with 1000 gates, keeping the same number of switching gates (100), the activity will be 10%, with the same dynamic power but with a leakage reduced by a factor of 10 due to the reduction of the total number of gates.

However, leakage issues do not mean that the reduction of dynamic power is a solved problem. The next three papers present interesting techniques to reduce dynamic power. The first paper, *Level Conversion for Dual-Supply Systems* Ishihara *et al.* presents an on-chip multi- approach with well-designed level-shifters. The next two papers on this topic will appear in the March, 2004, of issue this TRANSACTIONS. Among them, the first one *Power-Delay Product Minimization in High-Performance 64-bit Carry-Select Adders*, by Néve *et al.*illustrates the choice of low-power logic styles and basic digital cells by presenting the design of very fast 64-bit adders using branch-based logic and decomposed complex gates. The next paper, *DCG: Deterministic Clock Gating For Low-Power Microprocessor Design*, by Li *et al.* presents the application of clock gating to microprocessors. While these techniques are not new *per se*, these papers advance these techniques to improve significantly the speed and power consumption behavior.

The last four papers, also in the next issue, deal with system issues. Given that Systems-on-Chips (SoCs) will contain up to 100 different memories on a single chip, memory issues have to be addressed more intensively. Consequently, these papers focus on the memory system. The first paper, *Memory Energy Minimization by Data Compression: Algorithms, Architectures and Implementation* by Benini *et al.* proposes to compress the software in the main memory and to decompress it on the fly when fetching blocks of instructions from the on-chip cache. The second paper, *Power-Aware Data Structure Transformations for Embedded Software with Dynamic Data Accesses*, by Daylight *et al.*proposes to introduce data-structure transformations to reduce the memory accesses, achieving significant reduction in execution time and power consumption for multimedia applications. The third paper, *A CAM with Mixed Serial-Parallel Comparison for Use in Low Energy Caches*, by Efthymiou *et al.*proposes to use CAM structure for the tags of a cache memory, and the fourth paper, *Compiler-Directed Scratch Pad Memory Optimization for Embedded Multiprocessors*, by Kandemir *et al.* presents a compiler strategy to reduce off-chip data accesses in a four-processor chip, using an on-chip scratch pad memory.

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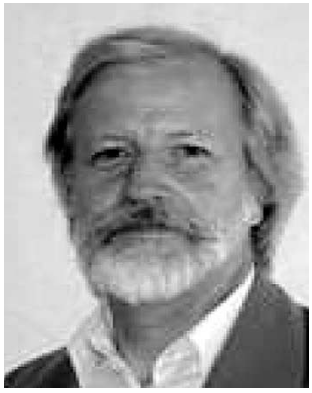
Digital Object Identifier 10.1109/TVLSI.2004.827390



Christian Piguet (M'03) was born in Nyon, Switzerland, on January 18, 1951. He received the M. S. and Ph.D. degrees in electrical engineering from the Ecole Polytechnique Fédérale de Lausanne, Switzerland, in 1974 and 1981, respectively.

He joined the Centre Electronique Horloger S.A., Neuchâtel, Switzerland, in 1974. He worked on CMOS digital integrated circuits for the watch industry, on low-power embedded microprocessors as well as on CAD tools based on a gate matrix approach. He is now Head of the Ultra-Low-Power Sector at the Centre Suisse d'Electronique et de Microtechnique S.A (CSEM), Neuchâtel, Switzerland. He is presently involved in the design and management of low-power integrated circuits in CMOS technology. His main research interests include the design of very low-power microprocessors and digital signal processing (DSP), low-power standard cell libraries and memories, low-power techniques, and asynchronous design. He is a Professor at the Ecole Polytechnique Fédérale Lausanne (EPFL), Switzerland, and also lectures in VLSI and microprocessor design at the University of Neuchâtel, Switzerland, and in the ALaRI Master at the University of Lugano, Switzerland. He is also a Lecturer for many postgraduate courses in low-power design. He holds about 30 patents in digital design, microprocessors, and watch systems. He is an author or coauthor of more than 150 publications in technical journals and of many books and book chapters in low-power digital design.

Dr. Piguet has served as a reviewer for many technical journals. He also served as Guest Editor for the July 1996 issue of IEEE JOURNAL OF SOLID-STATE CIRCUITS. He is a member of the steering and program committees of numerous conferences and served as Program Chairman of PATMOS'95 in Oldenburg, Germany, Co-Chairman at FTFC'99 in Paris, France, Chairman of the ACiD'01 Workshop in Neuchâtel, Co-Chair of VLSI-SOC'01 in Montpellier, France, and Co-Chair of ISLPED'02. He was Chairman of the PATMOS Executive Committee during 2002.

Vijaykrishnan Narayanan received the B.E. degree in computer science and engineering from the Sri Venkateswara College of Engineering (SVCE), University of Madras, Madras, India, in 1993 and the Ph.D. degree in computer science and engineering from the University of South Florida, Tampa, in 1998.

Since 1998, he has been with the Computer Science and Engineering Department at the Pennsylvania State University, University Park, where he is currently an Associate Professor. His research interests include energy-aware reliable systems, embedded Java, nano/VLSI systems, and computer architecture. He has authored more than 100 papers in these areas. His current research projects are supported by National Science Foundation, DARPA/MARCO Gigascale Silicon Research Center, Office of Naval Research, Semiconductor Research Consortium, and Pittsburgh Digital Greenhouse.

Dr. Narayanan served as General Chair for the IEEE Computer Society Annual Symposium on VLSI in 2003 and has served as the Treasurer for the International Symposium on Low-Power Electronics and Design since 2001. He has served on program committees of various conferences including HPCA, Design, Automation and Test in Europe (DATE), MSE, International Conference on Computer Design (ICCD), IEEE Computer Society Annual Symposium on Very Large Scale Integration (ISVLSI), International Symposium on Low Power Electronics and Design (ISLPED), ISPASS, HiPC, and GLSVLSI. He also serves as the Vice-Chair, Student Activities for the IEEE Computer Society and on the Student Activities Committee of IEEE. He has received several awards including the IEEE CAS VLSI TRANSACTIONS Best Paper Award in 2002, the Penn State CSE Faculty Teaching Award in 2002, the ACM SIGDA Outstanding New Faculty Award in 2000, National Science Foundation CAREER Award, Upsilon Pi Epsilon Award for Academic Excellence in 1997, the IEEE Computer Society Richard E. Merwin Award in 1996, and the University of Madras First Rank in Computer Science and Engineering Award in 1993 and Outstanding Student Award in 1987.