Guest Editorial

THIS Special Section of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS consists of extended versions of papers originally presented at the 2002 International Conference on Computer Design (ICCD) held in San Jose, CA, on October 13–15, 2002.

The ICCD encompasses a wide range of topics in the research, design, and implementation of computer systems and their components. The ICCD's unique multidisciplinary emphasis provides an ideal environment for developers and researchers to discuss practical and theoretical work covering system and processor architecture, logic and circuit design, verification and test methods, along with tools and methodologies.

A primary goal of ICCD was to present a technical program of the highest quality to its participants and bring together top researchers and developers from academic institutions, research laboratories, and high-technology companies from around the world. The 173 paper submissions came from 19 different countries. Of the 173 papers originally submitted to the conference, the program committee worked diligently to select 47 regular papers for presentation. The program committee invited the authors of the most well-received papers at the conference to submit extended versions for consideration in this Special Section. Upon careful review, the following five papers were selected, which appropriately reflect the broad multidisciplinary nature of the conference.

The first two papers consider hardware for encryption and compression. The paper by Nikara *et al.*, "Multiple-symbol parallel decoding for variable length codes" presents a multiple-symbol parallel variable-length decoding scheme, including an efficient hardware implementation. When applied to MPEG-2 standard benchmark scenes, an average of 4.8 codewords are decoded per cycle, resulting in the throughput of 106 million symbols per second. The paper by Morioka and Satoh, "A 10-Gbps full-AES crypto design with a twisted-BDD S-Box architecture" describes the design of a high-speed core for advanced encryption standard (AES) which runs at 780 MHz in a 0.13-μm CMOS process and achieves a 10-Gbps throughput. A critical hardware component that defies pipelining is the S-box and the authors propose a new architecture that reduces latency by a factor-of-two over previous implementations.

The ICCD always has a good representation of papers on new design methodologies and tools flows. The third paper "Designing an asynchronous microcontroller using Pipefitter" by Blunno and Lavagno, describes a design methodology and synthesis flow for asynchronous circuits that uses Verilog both as a specification language and as an intermediate format. This allows "standard" EDA tools to be used for most parts of the design process, including synthesis, simulation, and layout.

The fourth paper by Ishaq *et al.*, "Fitted Elmore delay: A simple and accurate interconnect delay model" describes an enhanced Elmore delay model for modeling the delay of *RC*-limited on-chip interconnect. The model boasts the same computation efficiency as the standard Elmore delay (for example, within the inner loop of wire sizing optimization) but with an average error of less than 0.8%.

The final paper in this Special Section by Liao *et al.*, "An efficient external-memory implementation of region query with application to area routing" describes very practical implementation issues in the design of wire routing software, issues important in the implementation of real CAD tools but often missing in published papers. Specifically, the paper describes a disk implementation of two-dimensional region query for use in a detail area router.

I would like to thank the authors for their efforts in preparing their manuscripts for inclusion in this TRANSACTIONS and the reviewers in providing very helpful feedback to the authors. Special thanks are also owed to Michael Pham and Prof. N. Ranganathan for their help in making this Special Section possible.

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From 1992 to 1997, he was a Research Staff Member and Manager in the VLSI Design Department, IBM T. J. Watson Research Center, Yorktown Heights, NY, where he was responsible for the design methodology for IBMs G4 S/390 microprocessors. Since 1997, he has been with Columbia University, New York, where he is now an Associate Professor. He also served as Chief Technology Officer of CadMOS Design Technology, San Jose, CA, until its acquisition by Cadence Design Systems in 2001. His current research interests include design tools for advanced CMOS technology, on-chip test and measurement circuitry, low-power design techniques for digital signal processing, low-power intrachip communications, and CMOS imaging applied to biological applications.

Dr. Shepard received the Fannie and John Hertz Foundation Doctoral Thesis Prize in 1992. While at IBM, he received Research Division Awards in 1995 and 1997. He was also the recipient of an National Science Foundation CAREER Award in 1998 and the IBM University Partnership Awards in 1998, 1999, 2000, and 2001. He also received the 1999 Distinguished Faculty Teaching Award from the Columbia Engineering School Alumni Association. He has been an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS and was the Technical Program Chair and General Chair for the International Conference on Computer Design in 2002 and 2003, respectively. He has served on the program committees for ICCAD, DAC, ISCAS, ISQED, GLS-VLSI, TAU, and ICCD.