Special Section on the 2001 International Conference on Computer Design (ICCD)

THIS SPECIAL SECTION of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) Systems consists of extended versions of papers presented at the 2001 International Conference on Computer Design held in Austin, TX, on September 23–26, 2001.

The International Conference on Computer Design (ICCD) encompasses a wide range of topics in the research, design, and implementation of computer systems and their components. ICCDs unique multidisciplinary emphasis provides an ideal environment for developers and researchers to discuss practical and theoretical work covering system and processor architecture, logic, and circuit design, verification and test methods along with tools and methodologies.

ICCD has a proud tradition of bringing together top researchers and developers from academic institutions, research laboratories, and high-technology companies from all over the world. The paper submissions in 2001 came from 18 different countries. Even though the conference was held only days after the shocking and inconceivable events of September 11th, participation was high and by employing remote conferencing, practically no talk had to be cancelled.

The great influence of on-chip cache on microprocessor performance becomes evident by the first two papers. The first paper by Heather Hanson *et al.* "Static energy reduction techniques for microprocessor caches" covers the power dissipation issue. The gain in microprocessor performance by increasing the capacity of on-chip caches comes at the price of increased static energy consumption due to subthreshold leakage currents. This paper compares different techniques for reducing static energy consumption of on-chip level-1 and level-2 caches. One technique employs low-leakage transistors (multithreshold-MTCMOS technique) in the memory cell. Another technique, power-supply switching, can be used to turn off memory cells and discard their contents. A third alternative is dynamic threshold modulation, which places memory cells in a standby state that preserves cell contents. Experiments on the energy/performance tradeoffs of these techniques show that dynamic threshold modulation achieves the best results for level-1 caches, whereas low-leakage transistors perform best for the level-2 cache.

The next paper "Address-free memory access based on program syntax correlation of loads and stores" by Lu Peng *et al.* deals with cache latency which can profoundly impact microprocessor performance in spite of advanced out-of-order execution techniques. One way to circumvent this cache latency problem is to predict load values at the onset of pipeline execution by exploiting either the load value locality or the address correlation of stores and loads. The paper describes a new load value speculation mechanism based on the program syntax correlation of stores and loads. Instead of establishing the store/load correlation during runtime, the proposed method establishes a small symbolic cache to capture existing syntax correlations and memory reference locality. The symbolic cache is addressed by the encoding content of store/load instructions to enable data accesses in the front end of the processor pipeline to shorten load-to-use latency.

The paper by McGregor and Lee proposes two new instructions, which can be used to efficiently complete an arbitrary bit-level permutation of an n-bit word with or without repetitions. Permutations with repetitions are rearrangements of an ordered set in which elements may replace other elements in the set and are useful in cryptographic algorithms. Using these instructions, cryptographers can design ciphers and hash algorithms that obtain a desirable level of diffusion more rapidly. As a result, less encryption rounds may be required to achieve adequate security, and the throughput of encryption algorithms could be significantly improved. With the two instructions, 64-bit permutations with repetitions of 4-bit or larger subwords can be completed in one instruction. It is also shown that the proposed instructions can improve the performance of the popular DES block cipher by at least 55% in constrained environments such as smart cards or low-power wireless devices.

High-speed digital design increasingly demands analog insight. In particular, interconnect response at high frequencies and crosstalk (both capacitive and inductive) can result in glitches on wires that can produce functional failures in receiving circuits. Most of these important effects are not addressed with traditional ATPG and BIST techniques, which are limited to the binary representation. In their paper "On-chip oscilloscopes for noninvasive time-domain measurement of waveforms in digital integrated circuits," Zheng and Shepard explore the feasibility of integrating simple sampling oscilloscopes on-chip to provide waveforms on selective critical nets for test and diagnosis. The oscilloscopes rely on subsampling techniques to achieve 10 p/s timing accuracy. High-speed samples from a successive approximation 8-bit ADC are combined to convert the waveforms into digital data that can be incorporated in the scan chain of the chip. The paper describes the design and measurements of a chip incorporating these oscilloscopes with a high-frequency interconnect structure in a 0.25-μm process.

The last paper by Yang and Seger "Introduction to generalized symbolic trajectory evaluation" deals with verification issues in microprocessor design. Symbolic trajectory evaluation (STE) is a lattice-based model checking technology based on a form of symbolic stimulation. It offers an alternative to "classical" symbolic model checking that, within its domain of applicability, often is much easier to use and much less sensitive to state explosion. The limitation of STE, however, is that it can

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only express and verify properties over finite time intervals. This paper presents a generalized STE that extends STE style model checking to properties over infinite time intervals. The power of STE is strengthened by introducing a form of backward symbolic stimulation. This generalization gives one the power to choose and adjust the level of model abstraction for a particular verification goal. A large-scale industrial memory design is used to demonstrate the practicality of the approach.

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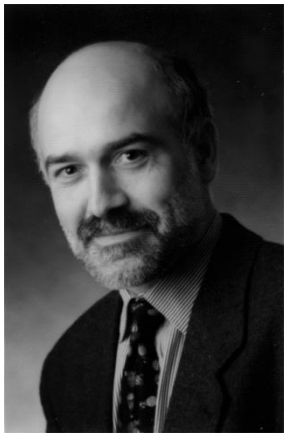

Yiannos Manoli (M'82) was born in Famagusta, Cyprus, in 1954. As a Fulbright scholar, he received the B.A. degree (*Summa cum laude*) in physics and mathematics from Lawrence University in Appleton, WI, in 1978, the M.S. degree in electrical engineering and computer science from the University of California, Berkeley, in 1980, and the Dr.-Ing. degree in electrical engineering from Gerhard Mercator University, Duisburg, Germany, in 1987.

From 1980 to 1984, he was with the University of Dortmund, Germany, working in the field of digital and analog MOS integrated circuit design with an emphasis on A/D and D/A converters. In 1985, he joined the newly founded Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany, where he established a design group for microsystem and microcontroller integrated circuits. His work there concentrated on mixed-signal CMOS circuits especially for monolithic integrated sensors such as surface micromachined pressure sensors, flow sensors, biosensors, etc. Another highlight of his work was the design of application specific microcontrollers as well as novel architectures and development tools for such microcontrollers. This work has resulted in several patents and over 60 technical publications. In September 1996, he joined the Department of Electrical Engineering, University of Saarland, Saarbruecken, Germany, where he held the Chair of Microelectronics. As Department Head he initiated a number of reforms that boosted the research activities and enhanced the teaching curriculum of the department. In 2000, he had the opportunity to spend half a year on a research project with Motorola in Phoenix, Arizona. In July 2001, he was appointed Chair of Microelectronics at the Institute of Microsystem Technology (IMTEK) of the Albert-Ludwig-University in Freiburg, Germany. His current research interests include the design of low-voltage/low-power mixed-signal CMOS circuits, sensor read-out and A/D- and D/A-Converters. For his patented work on a self-calibration method he received the Best Paper Award of the 14th "European Solid-State Circuits Conference" in 1980.

Prof. Manoli has served on the Committees of a number of conferences. In 2001, he was Program Chair and in 2002, General Chair of the IEEE International Conference on Computer Design (ICCD). He is a Member of Mortar Board, Phi Beta Kappa, and VDE.