Guest Editorial

THE SECOND part of this Special Section on Hardware/Software Codesign and System Synthesis covers a variety of topics in modeling, synthesis, and verification of mixed hardware/software systems. Part I of this Special Section appeared in the July 2006 issue of this TRANSACTIONS.

The first paper, "Retargetable pipeline hazard detection for partially bypassed processors" by A. Shrivastava, E. Earlie, N. D. Dutt, and A. Nicolau presents a compiler optimization technique that can significantly improve the instruction scheduling for processors with a partially bypassing datapath. Operation tables accurately describe the execution of an operation in the processor and help to avoid potential pipeline hazards.

The next two papers advocate scratchpad memories for embedded systems to reduce both energy usage and run-time, and offer techniques for utilizing them. In "Overlay techniques for scratchpad memories in low power embedded processors," M. Verma and P. Marwedel describe a scratchpad memory allocation technique for both instructions and variables that is 20% more energy efficient and exhibits 10% better performance than comparable unified caches. A. Janapsatya, A. Ignjatovic, and S. Parameswaran focus on instruction code in their paper "Exploiting statistical information for implementation of instruction scratchpad memory in embedded system." Based on a metric called concomitance, that captures the temporal relationships of instructions, a scratchpad allocation heuristic is presented that, on average, uses 41.9% less energy and improves performance by 40% when compared to an instruction cache.

The paper, "Expression equivalence checking using interval analysis," by M. A. Ghodrat, T. Givargis, and A. Nicolau addresses the problem of formally deciding if two arithmetic expressions are equivalent. The authors show that the domain space can be pruned substantially by means of interval analysis and fairly complex arithmetic expressions can be verified within seconds.

The next paper focuses on minimizing the area under timing constraints for soft real-time systems. In "Probabilistic delay budget assignment for synthesis of soft real-time applications" the authors, S. Ghiasi, P.-K. Huang, and R. Jafari, propose a time budget management technique based on the profiling of execution races, that relates expected system delay constraints to component time budgets. The paper reports an average area decrease of 17% for a core-based synthesis of a set of multimedia applications while meeting all soft real-time constraints.

System level modeling and design methodologies are as important as specific optimization techniques. S. A. Edwards and O. Tardieu propose in their paper "SHIM: A deterministic model for heterogeneous embedded systems," a deterministic, Kahn process network-based model with rendezvous communication to describe mixed hardware/software systems. They also describe a synthesis path to both hardware and software implementation of their model. In the last paper of this Special Section, J. M. Paul, D. E. Thomas, and A. Bobrek claim that the emerging class of heterogeneous multiprocessor systems are profoundly different from traditional full custom designs, from traditional general purpose designs, and from traditional real-time systems. In their paper "Scenario-oriented design for single-chip heterogeneous multiprocessors," they propose a design methodology that uses scenario-based benchmarking, where a scenario consists of a set of concurrent applications competing for resources. The paper illustrates how the perceived system performance heavily depends on the selected scenario and argues for systematic benchmarking and performance evaluation with scenarios drawn from real-life situations.

Finally, we would like to thank all the authors of the submitted papers, all the reviewers, the Editor-in-Chief Nagarajan Ranganathan, and Michael Pham for their high-quality contributions and all their efforts in making this Special Section possible. We have truly enjoyed working on this Special Section. We sincerely hope you also appreciate this slice of the state-of-the-art in hardware/software codesign and system synthesis and enjoy reading these stimulating articles.

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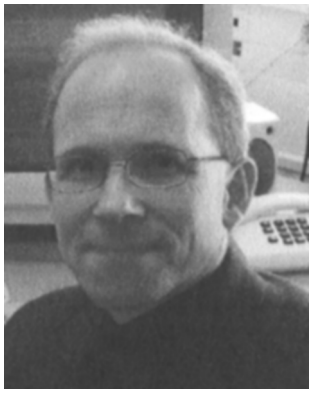

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