Editorial

THE 2003 International Workshop on System-Level Interconnect Prediction (SLIP) was the fifth such workshop and the fourth to have a special section devoted to it in the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS. SLIP exists to bring together researchers working in many areas related to interconnections who would otherwise not have a chance to interact. Specifically, interconnect is studied at a range of levels from technology to its impact on computer architecture or packaging issues. As an example, interconnect technologists tend to be isolated from researchers working on physical design, wire planning, IC microarchitecture, and other fields. However, it is exactly these groups of people that must interact to develop a cohesive and systematic approach to addressing the woes that interconnect is lately responsible for: these issues include signal integrity (coupling, both capacitively and inductively), delay, power consumption, yield, and chip density. SLIP has evolved over the past five years to include more and more of these topics while maintaining a distinct "prediction" personality. For instance, in the 2003 proceedings, there were several field-programmable gate-array (FPGA) oriented papers as well as efforts at post-Rentian analysis of wirelength distributions. SLIP'03 also brought in three invited speakers from distinguished industrial research labs (IBM, Intel, and Philips) to provide their perspective on issues ranging from the practical (how do current wirelength distribution models actually fit to real commercial chips?) to the more visionary (how can routability be captured and/or predicted at the logic synthesis stage of design?).

The first paper in this special section by Liu et al. integrates wirelength prediction into circuit placement. In particular, predicted wirelengths are used as constraints during the simulated annealing step of a placement algorithm. Within a timing-driven placement flow, the results show up to 11% better timing than when using a traditional placement flow that does not rely on wirelength prediction techniques. This paper serves as an example of ways in which recent work on improving wirelength prediction by the SLIP community can be used in the integrated circuit design flow.

The next group of papers all deal with interconnect prediction in field programmable gate arrays (FPGAs), which was one of the more prominent topics at the SLIP'03 workshop. The first paper by Anderson and Najm stresses the need for predicting power consumption due to interconnect in FPGAs. Since wires dominate in FPGAs, early prediction of the interconnect capacitance and switching activity will enable more accurate overall power estimation. The authors build models of capacitance and data activity by performing regression analysis on a range of circuits mapped onto a FPGA. The selection of the relevant input parameters to this model is one of the main contributions of the work. This work has implications in the areas of low-power FPGA synthesis, power-aware layout, and others. The second FPGA related work is by Yeh and Marek-Sadowska and discusses an approach to delay budgeting for sequential circuits that relies on retiming and verifies this approach in an FPGA placement flow. The authors formulate the problem as a linear programming problem to achieve an efficient solution and also propose new weighting functions based on wirelength to yield good budgeting results. The next paper dealing with interconnection in FPGAs is by DeHon and Rubin and attempts to answer the question: How should multilevel metallization affect the design of FPGA interconnect? The authors propose an alternate topology for FPGA interconnect that shows better scalability with larger number of metal layers than the traditional Manhattan-style interconnect structure. Rentian techniques are used to demonstrates this improved scalability and the ideas presented have far-ranging implications on FPGA design. A second paper by DeHon demonstrates that several conceptually different routing architectures useful for programmable logic exhibit the same asymptotic wiring requirements. The author describes upper and lower bounds on channel resource requirements and shows how to produce layouts in two-dimensional meshes that are within a constant factor of optimal.

The next paper by Davoodi *et al.* discusses an empirical approach to generating wirelength probability distributions that can then be leveraged throughout the design flow, whenever wirelength estimates are needed. The new model compares very favorably to standard half-perimeter bounding box models and is applied to the buffer insertion problem where wirelength probability distributions are used to maximize the likelihood that the delay constraint is met. In general, this paper can be seen as one of the earliest efforts towards a true probabilistic design flow (contrasting with today's traditional deterministic or corner-case based methodologies). The final paper, by Patel and Markov, investigates bus encoding schemes to make global on-chip buses more tolerant of crosstalk noise and other interference effects. With shrinking noise margins and a growing number of noise sources in digital systems today, the authors make an important contribution by addressing error correction and noise avoidance concurrently. Another interesting aspect of the paper is that it offers gate-level implementation suggestions for the encoding/decoding circuitry, which is commonly overlooked in the bus encoding literature.

In closing, we would like to thank the authors of the above papers for their contributions as well as the reviewers who spent many hours ensuring the quality of this special section. We also sincerely appreciate the efforts of Editor-in-Chief, Nagarajan Ranganathan and TVLSI administrative editorial assistant, Michael Pham, for supporting this special section on

Digital Object Identifier 10.1109/TVLSI.2004.836421

SLIP techniques. Interested readers are referred to www.sliponline.org for more details about the system-level interconnect prediction community.

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Dennis Sylvester (M'00) received the B.S. degree (*summa cum laude*) from the University of Michigan, Ann Arbor, in 1995, and the the M.S. and Ph.D. degrees, all in electrical engineering, from University of California, Berkeley, in 1997 and 1999, respectively.

From 1996 to 1998, he was with Hewlett-Packard Laboratories, Palo Alto, CA. He was also a Senior Research and Development Engineer with the Advanced Technology Group, Synopsys, Mountain View, CA. Currently, he is an Assistant Professor in the Department of Electrical Engineering, University of Michigan, Ann Arbor. He has published numerous articles in his field of research, which includes the modeling, characterization, and analysis of on-chip interconnect, low-power circuit design and design automation techniques, and variability-aware circuit approaches.

Dr. Sylvester received a National Science Foundation CAREER Award, the 2000 Beatrice Winner Award at ISSCC, two outstanding Research Presentation Awards from the Semiconductor Research Corporation, and a Best Student Paper Award at the International Semiconductor Device Research Symposium. His dissertation research was also recognized with the 2000 David J. Sakrison Memorial Prize as the most outstanding research in the Department of Electrical Engineering and Computer Science, University of California, Berkeley. He is the recipient of the 2003 ACM SIGDA Outstanding New Faculty Award and the 1938E Award for teaching and mentoring, which is the highest award given to a junior faculty at the Michigan College of Engineering. He has served on the technical program committee of numerous design automation and circuit design conferences and was General Chair for the 2003 IEEE System-Level Interconnect Prediction (SLIP) Workshop. He is an Associate Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS and is General Chair for the 2005 IEEE Workshop on Timing Issues in the Synthesis and Specification of Digital Systems (TAU). In addition, he helped define the circuit and physical design roadmap as a member of the International Technology Roadmap for Semiconductors (ITRS), U.S. Design Technology Working Group from 2001 to 2003. He is a member of ACM, American Society of Engineering Education, and Eta Kappa Nu.

Andrew B. Kahng was born in 1963, in San Diego, CA. He received the A.B. degree in applied mathematics (physics) from Harvard College, Cambridge, MA, and the M.S. and Ph.D. degrees in computer science from the University of California at San Diego.

From June 1983 to June 1986, he was with Burroughs Corporation Micro Components Group, San Diego, where he worked in device physics, circuit simulation, and CAD for VLSI layout. In July 1989, he joined the Department of Computer Science Department, University of California, Los Angeles, (UCLA), as an Assistant Professor, where in July 1994, he became an Associate Professor, and then a Full Pofessor in July 1998. From April 1996 to September 1997, he was on sabbatical leave and leave of absence from UCLA, as a Visiting Scientist at Cadence Design Systems, Inc, San Jose, CA. He resumed his duties at UCLA in Fall 1997, and from July 1998 to September 2000 served as the Computer Science Cepartment's Vice-Chair for graduate studies. Effective January 1, 2001, Professor Kahng joined University of California at San Diego, as Professor in the Computer Science Engineering and Electrical and Computer Engineering Departments. He has published well over 200 journal and conference papers. His research interests include the VLSI design-manufacturing interface, VLSI physical layout design and performance analysis, combinatorial and graph algorithms, stochastic global optimization, and (as the opportunity arises) other areas of applied algorithmics such as bioinformatics or computational commerce.

Prof. Kahng has received National Science Foundaton Research Initiation and Young Investigator Awards, eight best paper nominations, and DAC, ISQED, and ASP-DAC/VLSI Design Best Paper Awards. He was the founding General Chair of the 1997 ACM/IEEE International Symposium on Physical Design, Co-founder of the ACM Workshop on System-Level Interconnect Prediction, and defined the physical design roadmap as a member of the Design Tools and Test Technology Working Group (TWG) for the 1997, 1998, and 1999 renewals of the International Technology Roadmap for Semiconductors (International Technology Roadmap for Semiconductors. He has also served as a member of the EDA Council's EDA 200X task force, which produced this report. He has been Chair of the U.S. Design Technology Working Group, and of the Design International Technology Working Group, for the 2001 renewal, 2002 update, and 2003 renewal of the International Technology Roadmap for Semiconductors. He was Technical Program Chair of EDP-2001 (the workshop of the Electronic Design Processes Subcommittee of the IEEE DATC), and General Chair of EDP-2002. He was also on the steering committees of ISPD-2001/2002 and SLIP-2001. He is currently the Technical Program Co-Chair of the 2004 Design Automation Conference, and remains on the committees of ISPD, SLIP, and EDP, as well as on the editorial boards of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, and *IEEE Design and Test*.