Introduction to the Special Section on Nanocircuits and Systems

IT IS WITH great pleasure that we introduce the Special Section on "Nanocircuits and Systems" to the readership of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.

The objective of this Special Section is to cover the ever expanding topical area of nano-based computing to address circuit and system related topics that are affecting the overall design of complex integrated circuits. While at device level, advances in material and physics related phenomena are being investigated and proposed to superseed CMOS at the end of the Technology Roadmap, there has also been a large body of research to apply such structures to circuits and then integrate them into systems.

These developments are at the forefront of the electrical and computer engineering community by which scientific advances can be translated into commercial products through engineering solutions.

This Special Section consists of six papers that have been selected to cover a wide spectrum of techniques which are encountered in the design of circuits and system for nano-scale computing.

The first paper of this Special Section is titled "Fault Secure Encoder and Decoder for NanoMemory Applications," by Naeimi and DeHon, presents a novel lithographic-scale implementation for an encoder/decoder that results in multiple fault tolerance within the memory array as well as this important circuit itself. This is accomplished through the use of Euclidean geometry codes to permit fault-secure operation with respect to permanent and transient faults. Its contribution lies in the synergetic effects among these types of faults under the proposed codes and its comprehensive treatment using an elegant circuit arrangement at modest area overhead. An extensive analysis and simulation results are used to validate these findings.

In the second paper, "Tunneling-Based Cellular Nonlinear Network Architectures for Image Processing," Mazumder *et al.* use the negative differential resistance of a resonant tunneling diode (as basic device) to implement a compact nanoarchitecture. This architecture relies on cellular neural/nonlinear networks to process images at high speed. Different features (such as stability, driving-point-plot analysis, and settling time) are considered at circuit-level to demonstrate the viability of this approach to implement a full array simulation of a 128×128 system. Moreover, it shows that the proposed nanoscale implementation is superior to CMOS over a wide range of performance metrics for many image processing applications.

In the third paper of this Special Section, "Application Exploration for 3-D Integrated Circuits: TCAM, FIFO, and FFT Case Studies," Davis *et al.* present a detailed assessment of 3-D stacking and integration through the use of drivers and CAD. This paper shows that memory and interconnect-based applications and circuits can substantially benefit from this type of architectures. Three real case studies are analyzed in detailed using the 3-D topology. It is particularly impressive that the benefits of 3-D integration need an accurate evaluation and analysis to fully utilize these capabilities in real life circuits.

The next paper included in this Special Section is "Analyzing the Inherent Reliability of Moderately Sized Magnetic and Electrostatic QCA Circuits Via Probabilistic Transfer Matrices," by Dysart and Kogge. Quantum-dot cellular automata (QCA) has received considerable attention as it may offer high device density while achieving significant improvement in performance compared to nano-CMOS. This paper concentrates on the reliability of two types of QCA circuits, namely those manufactured using electrostatic and magnetic devices. By using linear regression (at considerable savings in computation), sensitivity to faults has been identified; probabilistic transfer matrices are then employed to provide a framework by which reliability can be improved at the critical circuit level. It is shown that for both types of QCA implementation, the interconnect represents a significant reliability bottleneck. The authors suggest different arrangements for the QCA interconnect by which substantial improvement in operational reliability can be achieved.

The fifth paper is "A Novel Adaptive Design Methodology for Minimum Leakage Power Considering PVT Variations on Nanoscale VLSI Systems," by Kim and Kim. This paper considers a very important metric of VLSI system, namely the power dissipation encountered at nanoscales due to leakage currents especially in standby mode. The novelty of the proposed technique is the adaptive nature by which process, voltage, and temperature (PVT) variations are taken into consideration, mostly at circuit level (through scaling of supply-voltage and body-bias-voltage) at the reduced features sizes of nano-CMOS. Extensive simulation results on combinational benchmark circuits are provided by which the proposed (monitoring) implementation is applied to show that it provides a realistic alternative solution as design methodology.

The sixth and last paper is titled "Analysis of Defect Tolerance in Molecular Electronics," by Dai *et al.*, deals with the pressing concern of manufacturing defects and their impact on the design of molecular electronics through a redundancy-based arrangement.

Differently from previous works, the proposed approach exploits a very singular yet powerful similarity between information processing and defect tolerance. This approach relies on a theoretical framework by which delivery of information through a "lossy" medium can be utilized to establish the gap in reliability between redundancy-based defect tolerance and the ideal organization of molecular systems (such as nanocrossbars) for post-CMOS technology. The analysis is pursued to establish the reliability bound such that design optimization can then take

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place for determining the level of defect tolerance that is required for system operation and manufacturing.

We sincerely hope that this Special Section will be a reference publication for future research. The topics covered in the papers are timely and important, and the authors have done an excellent job of presenting the material. We extend our sincere thanks to all the authors and reviewers. We also thank Dr. N. Jha Editor-In-Chief of IEEE TVLSI for allowing us to have this Special Section. Finally, a special thanks is due to all the staff for editing and assembling it. Please feel free to contact us if you have questions or comments.

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