Special Section on International Symposium on Networks-on-Chip (NOCS)

NETWORK-ON-CHIP (NoC) is an emerging paradigm using packet-switched networks for communications within large VLSI systems on-chip. NoCs are poised to provide enhanced performance, scalability, modularity, and design productivity as compared with previous communication architectures such as busses and dedicated signal wires. With the emergence of large numbers of cores in general-purpose and systems-on-a-chip (SoCs), NoCs are likely to be the prevailing on-chip interconnect fabric.

The idea for this special section started with the intention to archive the top papers from the First ACM/IEEE International Symposium on Networks on Chips (NOCS) in 2007, a premiere venue for architectural, circuits, and design research into NoCs. NOCS came about with a vision to establish a new research community that straddles traditional research area boundaries and encompasses research from diverse disciplines such as computer architecture, CAD, general networking, VLSI design, and process technology amongst others.

We solicited and received 29 submissions in December 2007, with each paper assigned to at least 4 reviewers. After going through four rounds of deliberations between the guest editors and the reviewers, we arrived at the final six papers accepted here.

Networking concepts from the domains of telecommunications and parallel computers do not apply directly on chip. From a networking perspective, they require adaptation because of the unique nature of VLSI constraints and costs: e.g., area and power minimization are essential; buffer space in on-chip switches is limited, latency is very important, etc. At the same time, there are new degrees of freedom available to the network designer, such as the ability to modify the placement of network endpoints. From the viewpoint of a VLSI designer, many well-understood problems in the realm of chip development methodology get a new slant when they are formulated for a NoC-based system, and new tradeoffs need to be comprehended. Therefore, the field offers opportunities for novel solutions in network engineering as well as system architecture, circuit technology, and design automation. The papers in this special section reflect the current exploratory state of research, where a new environment has created modifications in many known problems. Hence, a large solution space needs to be surveyed from new and different perspectives.

The first two papers tackle the tight power constraints of on-chip network design. In the paper "An Energy and Performance Exploration of Network-on-Chip Architectures," Banerjee et al. compare several router architectures in terms

of power and performance, using 90-nm CMOS library cells for system implementations and employing a set of streaming traffic conditions for evaluation. The paper "Design and Management of Voltage-Frequency Island Partitioned Networks-on-Chip" by Ogras et al., proposes a methodology to design a NoC-based GALS system with multiple clocks and voltage islands. A field-programmable gate-array (FPGA) prototype with a real video application was used for validation of the system architecture described in this paper.

The next two papers tackle routing protocol design in the face of VLSI constraints of area and floorplanning. The paper "Custom Networks-on-Chip Architectures with Multicast Routing" by Yan and Lin, revisits classical problems of VLSI physical design, such as floorplanning and routing, and reformulates them for the NoC-based design paradigm. The proposed design process consists of partitioning traffic flows into sets, and generating physical network topologies with rectilinear Steiner trees. Further optimization is proposed at the NoC level, such that message routing is deadlock-free for both unicast and multicast traffic. Another paper which addresses NoC routing is "Region-Based Routing: A Mechanism to Support Efficient Routing Algorithms in NoCs." Mejia et al. propose to avoid the usage of routing tables in network switches, since such tables are considered unsuitable for residing within on-chip routers due to area constraints. Instead, a region-based routing mechanism is proposed, which implements the routing function with logic blocks.

Finally, two papers present case studies of real NoC-based chip implementations. In the paper "81.6 GOPS Object Recognition Processor Based on Memory-Centric NoC," Kim et al. describe a specialized parallel processor for a dedicated image processing application, implemented in 180-nm technology. Ten processing elements exchange data via eight specialized memory arrays using an optimized NoC, achieving high performance at low power. In "A Case Study for NoC-Based Homogeneous MPSoC Architectures," by Tota et al., a 90-nm implementation of a 16-processor NoC-based system is described and evaluated for a ray tracing graphic application.

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