Guest Editorial Special Section on Low-Power Electronics and Design

THIS ISSUE of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATED (VLSI) SYSTEMS features a Special Section on Low-Power Electronics and Design, which highlights some of the best papers that have been published in the *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, Tegernsee, Germany, October 4–6, 2006. Out of more than 40 submissions received from experts in the field for this Special Section, and after more than 100 reviews, only eight manuscripts could be accepted to be included in this issue. These eight papers cover various areas related to low-power electronics and design, ranging from circuit and design technology to system level power modeling and optimization.

Starting from the lowest levels of abstraction, the paper "Robust multiple-phase switched-capacitor DC–DC power converter with digital interleaving regulation scheme," by Ma and Luo, proposes an integrated switched-capacitor (SC) DC–DC converter with a digital interleaving regulation scheme. By interleaving newly-structured charge pump (CP) sub-cells in multiple phases, the input current ripple and output voltage ripple are reduced significantly. One of the main features of the proposed scheme is reliability, indeed, the converter exhibits excellent robustness, even when one of the CP sub-cells fails to operate. To achieve fast transient response, hysteretic control is adopted in the controller. The design provides a high performance solution for new generation, robust on-chip power supply designs. The second paper, "Novel video memory reduces 45% of bitline power using majority logic and data-bit reordering," by Fujiwara *et al.*, addresses the problem of a low-power two-port SRAM for video processing which is shown to consume 45% less power on the read bitline in a 90-nm process technology. The idea is based on a novel two-port SRAM design using majority logic and data-bit reordering. The proposed SRAM is suitable for real-time image processing for statistically similar data and provides a total power reduction of 28% with only 4% hit in performance and 7% area overhead.

Four additional papers focus on low-power issues at the micro-architectural abstraction level and the system level. Starting with the first group, the paper entitled "L-CBF: A low-power, fast counting bloom filter architecture," by Safi *et al.*, targets to improve the power-delay product by deploying hardware counting bloom filters (CBFs). Investigated are two implementations of CBFs in a 130-nm technology. The major results the authors report are twofold. First, the proposed CBF using an array of up/down linear feedback shift registers and local zero detectors may lead to a 3.7× faster and 1.4× lower energy design compared to an SRAM-array-based design. Second, the authors present architectural analytical energy and delay models for various CBF organization that are shown to be within 10% or even 5% compared to physical models. The second micro-architecture-level paper, "Dynamic thermal clock skew compensation using tunable delay buffers," by Chakraborty *et al.*, addresses the idea of dynamically modifying the clock tree with the aim to compensate temporal variations of the temperature. In this context, buffers inserted in the clock tree are used as tunable delay elements. The core of the paper is a synthesis algorithm that minimizes the number of inserted buffers such that the incurred overhead in worst-case power and area is with 3.5% and 5.5% bounds, respectively.

At the system level, the paper "Selective writeback: Reducing register file pressure and energy consumption," by Balkan *et al.*, addresses the problem of large register files which are needed in speculative computation to maintain results until a point where these results can be safely discarded. The energy consumed in these registers contribute to a significant amount of the energy consumption. Investigation of Balkan *et al.* unveiled that about 45% of the time, the values in these registers are actually never read from since the respective values are carried to the consumers via a bypass network. The paper is therefore targeted for identifying those cases and consequently to avoid a writeback of such transient values. Balkan *et al.* report an 11% performance increase when applying their technique and a 29% reduction in register file energy. Another paper, "GOP-level dynamic thermal management in MPEG-2 decoding," by Lee *et al.*, deals with a dynamic thermal management algorithm in order to achieve a thermally safe state of operation. Their technique is applied to an MPEG-2 video decoding application. Their algorithm uses dynamic voltage and frequency scaling under the constraint of frame-rate-dependent group-of-pictures deadline. More specifically, Lee *et al.*'s approach satisfies the given temperature and performance constraints, while guaranteeing minimal energy consumption of the microprocessor.

Two short papers also target design and circuit technology issues related to low-power design. To this end, "Self-timed regenerators for high-speed and low-power on-chip global interconnect," by Singh *et al.*, addresses the important problem of improving the power (and speed) of on-chip global interconnects. Singh *et al.* propose new circuit blocks called self-timed regenerator (STR) which are placed along global wires to compensate the loss in resistive wires and to amplify the effect of inductance in the wires to enable transmission line like behavior. In 90-nm CMOS technology, STR design achieved a delay improvement of 14% over the conventional repeater design, with 20% power reduction for the same delay, and 8% delay improvement for the same power when compared with the repeater design. A second short paper "A current-recycling technique for shadow-match-line sensing in content-addressable memories," by Zhang *et al.*, proposes a current-recycling technique for shadow-match-line (SML) sensing in content-ad-

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dressable memories (CAMs). To minimize energy-overhead, a novel current-recycling voltage detector (CRVD) is devised, whose working current is reused to charge up the match-line (ML) to determine matches or mismatches. With this CRVD, the word circuits realize fast-disable of the charging paths in case of mismatches. Prelayout simulation results show the proposed 256-word $\times$ 144-bit ternary CAM, based on a 0.13-μm 1.2-V CMOS process, achieves 0.51 fJ/bit/search for the word circuit with less than 900-ps search time or a 74.2% energy-delay-product (EDP) reduction as compared with the speed-optimized current-saving scheme. Post-layout simulation confirms the features of the design, with 0.65 fJ/bit/search energy per search with 1.2-ns search time.

Summing up, this Special Section covers a wide area of low power related research papers ranging from circuit/device level to system level techniques and architectures. The selected papers cover very promising approaches and techniques for achieving low power at varying levels of abstraction. We hope the readers will find this Special Section intellectually satisfying, while also opening new directions in low-power electronics and design.

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