Guest Editorial Special Section on Design Verification and Validation

THE VERIFICATION and validation problems associated with complex hardware designs are significant and costly. Unlike in the software marketplace, hardware design errors are not tolerated. With growing design complexities, such high standards are increasingly difficult to meet. The papers in this Special Section span a wide range of critical topics in verification including microprocessor validation, simulation-based equivalence checking, system-on-chip (SoC) verification, test generation, and fault emulation.

Microprocessor verification is consistently an important research area. A modeling framework for microprocessor design and validation is presented in "MMV: A metamodeling-based microprocessor validation environment," by Mathaikutty *et al.* The modeling framework is UML-based and allows the definition of relationships between descriptions at different abstraction levels. The framework also supports the generation of test constraints, which can be satisfied using a constraint solver to generate tests. A compositional verification approach for pipelined processors is presented in, "A refinement-based compositional reasoning framework for pipelined machine verification," by Manolios and Srinivasan. Well-founded equivalence bisimulation refinement is used to prove equivalence between an instruction set architecture and a machine architecture.

The next two papers in this Special Section explore solutions to the equivalence checking problem using simulation rather than formal methods. The work presented in "Novel probabilistic combinational equivalence checking," by Wu *et al.*, determines equivalence between two gate-level circuits by simulating the circuits with a weighted random pattern sequence and then comparing the output signal frequencies. It is possible that two non-equivalent circuits have the same output signal frequencies, so the challenge is to select weights on the input sequence which reduce the aliasing probability. A related problem, checking equivalence between a behavioral and a register–transfer level (RTL) description through simulation, is addressed in "Simulation bounds for equivalence verification of polynomial datapaths using finite ring algebra," by Shekhar *et al.* This research demonstrates that exhaustive simulation is not necessary to prove equivalence. Shenkar *et al.* also derive a theoretical upper bound on the number of vectors required to prove equivalence.

Several papers focus on different aspects of the SoC verification problem. The difficulty of skew minimization in clock routing makes totally synchronous design practically impossible in SoCs. Detection of synchronization-related errors in SoCs is investigated in, "Validating Power Architecture Technology-based MPSoCs through executable specifications," by Bhadra *et al.* By comparing the RTL simulation trace to a trace generated by an abstract C++ behavioral description, synchronization issues such as barrier orders, mutual exclusion, and cache coherency can be evaluated. The IEEE 1500 Standard is used to alleviate SoC testing problems by defining a common test wrapper which can be used to access deeply embedded core components. The standard specifies the behavior of the wrapper while allowing core vendors flexibility in the design process. The paper, "IEEE Standard 1500 compliance verification for embedded cores," by Benso *et al.*, outlines the testing requirements to guarantee that a wrapper design is compliant with the IEEE 1500 Standard.

Test generation and fault simulation are fundamental testing problems and are addressed in this Special Section. A behavioral test generation technique is presented in, "Automatic constraint-based test generation for behavioral HDL models," by Hari *et al.* Test constraints are extracted from the behavioral code and are satisfied using a constraint solver to generate tests. Fault simulation, the process of simulating faulty versions of a design, is often used to determine the resilience of a design to errors. The process is typically time consuming due to the large number of faults evaluated. The research presented in, "Fault emulation for dependability evaluation of VLSI systems," by de Andres *et al.*, employs emulation to greatly accelerate the process.

We hope that this Special Section will be an important source of information about current issues in design verification. Please enjoy the issue!

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He is currently an Associate Professor with the Computer Science Department, University of California Irvine, Irvine. From 1997 until June 2003, he was a member of the faculty in the Electrical and Computer Engineering Department, University of Massachusetts, Amherst. His research interests include the test and validation of hardware and software systems. His current research projects include testing for software security and hardware/software covalidation.

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Dhiraj Pradhan currently holds a Chair in the Department of Computer Science, University of Bristol, Bristol, U.K. Before this, he was a Professor with the Department of Electrical and Computer Engineering, Oregon State University, Corvallis. Previous to this, he held the COE Endowed Chair Professorship with the Computer Science Department, Texas A&M University, College Station, where he also served as founder of the Laboratory of Computer Systems. Prior to this, he held a Professorship with the University of Massachusetts, Amherst, where he also served as Coordinator of the Department of Computer Engineering. He has also worked with the University of California, Berkeley, Oakland University, Rochester, MI, and the University of Regina, Saskatchewan, Canada, and as a Visiting Professor with Stanford University, Stanford, CA. In the past, he worked as a Staff Engineer with IBM, more recently serving as the founding CEO of Reliable Computer Technology, Inc. He is also the inventor of two patents, one of which was licensed to Mentor Graphics and Motorola. The recently-announced verification tool, Formal Pro, by Mentor Graphics is based on his patent. He has contributed to VLSI computer-aided design and test, as well as to fault-tolerant computing, computer architecture, and parallel processing research, with major publications in journals and conferences, spanning more than 30 years. During this long career, he has been well-funded by various agencies in Canada, USA, and U.K. He has also served as coauthor and editor of various books, including *Fault-Tolerant Computing: Theory and Techniques, Vols. I & II* (Prentice-Hall, 1986), *Fault-Tolerant Computer Systems Design* (Prentice-Hall, 1996, 2nd print 2003), and *IC Manufacturability: The Art of Process and Design Integration* (IEEE, 2000).

Prof. Pradhan was a recipient of Best Paper Awards honors including the 1996 IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS Best Paper Award, with W. Kunz, on "Recursive Learning: A New Implication Technique for Efficient Solutions to CAD Problems Test, Verification, and Optimization," was also the recipient of a Humboldt Prize, Germany, and the Fulbright-Flad Chair in Computer Science in 1997. He continues to serve as an Editor in prestigious journals, including IEEE TRANSACTIONS. Further, he has worked as an editor for several journals, including IEEE TRANSACTIONS and JETTA. Also, he has served as General Chair and Program Chair for various major conferences. He is also included among 230 computer scientists worldwide whose work has been highly cited in the list appearing in www.isihighlycited.com. He is a fellow of the Association of Computing Machinery (ACM) and the Japan Society of Promotion of Science.