Guest Editorial
Special Section on Configurable Computing Design— I: High-Level Reconfiguration

CONFIGURABLE computing, also called reconfigurable or adaptive computing, is a fast growing area in digital design and computer engineering. The reason is that the traditional market of microelectronics is shifting from industrial to consumer application. The main driving forces have been mobile computing and automotive industry. In these application areas, the traditional approaches, based on microprocessors and/or application-specific integrated circuits (ASICs), do not work well. These applications need flexible, high-performance devices with low power consumption. Microprocessors are too slow and energy hungry while ASICs are efficient but inflexible. Thus, the new emerging applications and market demand new technology. Many companies and researchers believe that the answer will be configurable computing platform. Recent developments show that configurable computing can outperform traditional, microprocessor-based solutions 10–100 times.

In the early years, the reconfigurable computing platform was used in very dedicated and specific application areas: in specialized signal and image processing systems and for prototyping VLSIs for embedded systems. Today, the reconfigurable computing platform is used for a wide range of applications: from very dedicated embedded applications to supercomputing. The range of research problems and interests runs from purely hardware related designs to building multiprocessing systems on reconfigurable spaces of elementary processors; from fine-grain granularity and parallelism to coarse-grain parallelism.

The new emerging areas of consumer microelectronics are mobile handheld appliances (handheld devices, multimedia, and communication systems); computer networking; mobile vehicular systems (automotive applications with embedded control systems, communication systems and multimedia); supercomputing applications and configurable multiprocessors. During the past years, the security related problems on configurable computing platform has gained particular interest.

Thus, the configurable computing forms a new and complete field in digital engineering, covering theory and applications, hardware, and software.

This Special Section on Configurable Computing Design covers physical, purely hardware related designs level as well as abstract level: building flexible and adaptable multiprocessing environments with operating systems, often heterogeneous systems containing fine-grain configurable components and reconfigurable multiprocessing environments (MPSoCs).

We received 98 submissions from which 16 papers were selected for publishing. These papers are divided between two Special Section issues, both containing eight papers. Issue I,

"High-Level Reconfiguration" and issue II, "Hardware Level Reconfiguration."

The first issue on "High-Level Reconfiguration" deals with arranging computational processes on a configurable hardware platform: with problems above electronics. Nevertheless, it is not organizing computations in a traditional, von Neumann computer; it is implementing algorithms and computational processes directly in hardware. Dealing with configurable computing systems design issues, the gap between hardware and software is rather small. Configurable computing introduces traditional software related topics, such as languages, operating systems, and integrates these with hardware related topics of digital design. While in general, there is a similarity in theoretical models and methods on the functional level, the actual methods involved are rather different and need more specific attention from researchers.

The first two papers present coarse-grained reconfigurable processor architectures, which can be considered as reconfigurable multiprocessors, or multiprocessor systems on chip (MPSoC). Both these architectures present heterogeneous systems. The first paper, "Towards Software Defined Radios using Coarse-Grained Reconfigurable Hardware," by G. K. Rauwerda et al., deals with implementing mobile wireless terminals on reconfigurable MONTIUM tile processor. Wireless terminals are adaptive multimode communication devices. The implementation of these devices requires flexible and efficient hardware, which is provided by a heterogeneous reconfigurable architecture. The implementation of a WCDMA and an OFDM receiver in the same reconfigurable processor is discussed.

In "A Medium-Grain Reconfigurable Architecture for DSP: VLSI Design, Benchmark Mapping, and Performance," M. J. Myjak and J. G. Delgado-Frias present medium-grain reconfigurable architecture that combines the advantages of both: fine-grain flexibility of gate arrays and coarse-grain efficiency of word-length computations. They analyze the implementation of several common benchmarks, ranging from floating-point arithmetic to a radix-4 fast Fourier transform.

The next three papers deal with process management (or threads and tasks) in reconfigurable multiprocessor systems. These papers consider run-time process management strategies in heterogeneous system; present a new parallel programming model for reconfigurable computing; and energy efficient management of tasks in reconfigurable multiprocessing environment. All three papers can be classified as process management in configurable multiprocessing environment.

The first paper of this group, "Run-Time Management of a MPSoC Containing FPGA Fabric Tiles,'' by V. L. Nollet et al., deals with a heterogeneous multiprocessor system on reconfigurable hardware platform for multimedia applications. In such

systems, the run-time assignment of tasks onto the communication and computation resources of a reconfigurable multiprocessor becomes inevitable. This paper presents a run-time task assignment heuristic that provides fast and efficient task assignment in an MPSoC containing fine-grain reconfigurable hardware tiles.

The paper, "Achieving Programming Model Abstractions for Reconfigurable Computing," by D. Andrews *et al.*, introduces a programming model for specifying parallel threads running on a reconfigurable computing platform of hybrid CPU/FPGA system. The thread model abstracts the components on either side of the CPU/FPGA boundary into a unified, custom, threaded, multiprocessor architecture platform. This approach enables the use of standard thread communication and synchronization operations across the software/hardware boundary.

In the last paper of this group, "A Cooperative Management Scheme for Power Efficient Implementations of Real-Time Operating Systems on Soft Processors," by J. Ou and V. K. Prasanna, the process management in a real-time operating system is considered. This paper addresses energy efficiency in a system of FPGA-based configurable soft processors, which is achieved using configurability of soft processors and managing interrupts and tasks. The implementations of two popular real-time operating systems on a state-of-the-art FPGA device are presented.

The next two papers consider parallel processing applications on a reconfigurable computing platform. Both deal with network flow or traffic: one in computer network and the other in metropolitan road traffic network. The last one is also an example of using configurable computing platform for speeding up traditional supercomputing applications in science and engineering.

In the paper "Reconfigurable Architecture for Network Flow Analysis," S. Yusuf *et al.*, deal with parallel processing in analyzing network traffic in increasingly high network data rates. The multiple network flows are analyzed and processed in parallel using FPGA-based reconfigurable computing platform. This architecture can support flows at multigigabit rate, which is faster than most software-based solutions where acceptable data rates are typically no more than 100 million bits/s.

The paper "A Case Study of Hardware/Software Partitioning of Traffic Simulation on the Cray XD1," by J. L Tripp *et al.*, presents a case study of a simulation of metropolitan road traffic networks. The problem is mapped onto a reconfigurable supercomputer, the Cray XD1. Five different methods are presented for mapping the application onto the combined hardware/software system. The results show that key predictors of performance are not necessarily maximum parallelism, but must account for the fraction of the problem that runs on the reconfigurable logic and the amount data flow between software and hardware.

The last paper of this Special Section brings us back to the hardware architecture. "The Reconfigurable Instruction Cell Array," by S. Khawam *et al.*, presents an instruction cell-based reconfigurable computing architecture for low-power applications. Top-down software driven approach is used for development such array. Results show that it delivers considerably less power consumption when compared to leading VLIW and low-power DSPs processors, but still maintaining their throughput performance.

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Toomas P. Plaks (M'95) received the Ph.D. degree in computer engineering from Chalmers University of Technology, Gothenburg, Sweden, and the M.Eng. degree in computer engineering and information processing from Tallinn Technical University, Tallinn, Estonia.

He is the Managing Director and the founder of a newly established company, Conhard Design Ltd., London, U.K., in the area of mobile computing applications and hardware. He is also a Visiting Fellow of the Reading University, Reading, U.K., and the London South Bank University, London, U.K. His research interests include the design of high-performance application-specific processors, massively parallel computer systems, and reconfigurable architectures in mobile computing and multimedia applications. His main interests focus on the theory and design of regular processor arrays and mapping algorithms onto space and time, i.e., into hardware. Also, his interests include computer networking, mobile computing, and web-based technologies. He has published over 70 scientific papers including a monograph on a synthesis of regular processor arrays. He is the founder and the Chairman of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA) in Las Vegas, NV, and the initiator of Mobile Computing Hardware Architecture (MOCHA) Symposium, HI. He is the Guest Editor of a series of special issues on designing dedicated processors on reconfigurable computing platform.

Dr. Plaks is a member of the New York Academy of Sciences and the U.K. Chapter of the Association for Computing Machinery Special Interest Group on Design Automation (ACM SIGDA). His biography is included in the Marquis *Who's Who in Science and Engineering*.