Guest Editorial
Special Section on System-on-Chip Integration: Challenges and Implications

SYSTEM-ON-CHIP (SOC) is the term used for a fully integrated circuit (IC), where few if any additional electronic components are required to make a complete system. The term has had many and varied definitions over time. Today, a typical SOC IC can be anything from a complex mixed-signal product, where a wide range of functionality such as RF, analog, power management, and digital coexist on-chip, to a complex digital-only product. It can contain high current and/or high voltage outputs and precision operational amplifiers and detectors.

It is thus apparent that virtually every IC development can be incorporated under the SOC umbrella. The IEEE System-on-Chip Conference (IEEE-SOCC), currently in its 26th year, covers the majority of areas of possible integration in its technical program. This Special Section is partially based on a selection of papers submitted to the 2006 IEEE-SOCC, which have been extended and revised. Due to the intense interest in the subjects of this Special Section, additional submissions not connected to the IEEE-SOCC have also been included.

A total of 38 high-quality submissions have been considered for this Special Section. Reducing this Special Section down to these nine included papers has been a difficult task. The guest editors would like to acknowledge the 2006 IEEE-SOCC Track Chairs and the Technical Program Chair Dr. Thanh Tran. We are also highly indebted to the IEEE-TVLSI reviewers and the Editorial Board, for the success of this Special Section. Contributions ranging from emerging research in the SOC area to designs that advance specific aspects of SOC implementation, all the way to complete circuit design, are included in these nine papers.

Interconnect aspects are addressed in the first two papers, "Utilizing Redundancy for Timing Critical Interconnect," by Hu *et al.* and "3-D Topologies for Networks-on-Chip," by Pavlidis and Friedman. Timing performance and tolerance to open faults and variations is the focus of the first paper. In the second paper, topologies that develop from merging networks-on-chip (NoCs) with 3-D circuits are explored and innovative 3-D topologies proposed. Latency and power models describing these topologies are developed and used in an assessment of optimal power consumption and speed.

In "Applying CDMA Technique to Network-on-Chip," Wang *et al.* focus on achieving data-transfer concurrency eliminating data transfer latency variances caused by packet routing in a point-to-point NoC.

The focus of "An On-Chip Multichannel Waveform Monitor for Diagnosis of Systems-on-a-Chip Integration," by Noguchi *et al.* is on an on-chip multichannel waveform monitor in terms of power supply and signal integrity in analog and digital circuits in mixed-signal systems-on-chip integration, enabling on-chip diagnosis. The monitor, implemented in a 0.18-μm CMOS prototype chip, is described.

A statistical approach to synthesize an energy conscious custom bus architecture in the presence of random on-chip data traffic is described in "Simultaneous On-Chip Bus Synthesis and Voltage Scaling Under Random On-Chip Data Traffic," by Pandey and Glesner. A tradeoff between communication bus cost and energy consumption is explored.

A robust, scalable dual-clock first-input first-output (FIFO) architecture is described in the paper "A Scalable Dual-Clock FIFO for Data Transfers Between Arbitrary and Haltable Clock Domains," by Apperson *et al.* The architecture is demonstrated in a 0.18-μm CMOS design, showing to operate at 580 MHz with 10.3-mW power dissipation while performing simultaneous FIFO READ and WRITE operations.

A design-for-testability (DFT) method that accounts for both internal gate feedback and global completion detection feedback is described in "DFT Techniques and Automation for Asynchronous NULL Convention Logic Circuits," by Satagopan *et al.* The method has been fully automated and integrated into a commercial CAD tool suite.

SOC yield is addressed in "ProTaR: An Infrastructure IP for Repairing RAMs in System-on-Chips," by Huang *et al.*, where an infrastructure IP for repairing embedded memories is described. Various redundancy allocation algorithms can be performed such that improved repair rate for each defective memory can be obtained.

In the final paper of this Special Section, "Wafer-Level Modular Testing of Core-Based SOCs," by Bahukudumbi and Chakrabarty, a modular test method used for core-based SOC designs is described. The problem of selecting an appropriate number of test patterns for each embedded core such that the defect screening probability is maximized for a given upper limit on wafer-level test time, is formulated and solved.

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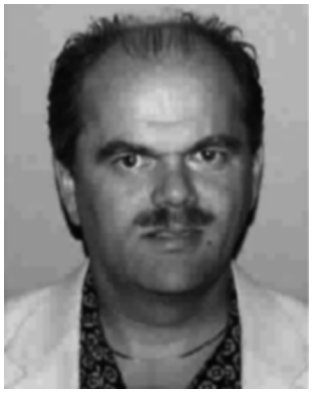

Radu M. Secareanu (M'00) received the Ph.D. degree from the University of Rochester, Rochester, NY, in 2000, previously working for five years as a design R&D Engineer.

Since 2000, he has been with the Microwave and Mixed-Signal Technologies Laboratory, Freescale Semiconductor (formerly Motorola SPS), Tempe, AZ. Since 2002, he has also been an Adjunct Professor with the Electrical Engineering Department, Arizona State University, Tempe. His research interests include signal integrity (substrate, interconnect, power-ground network) and the relationship with new technologies and mixed-signal and RF circuit design aspects, and low-voltage and low-power circuit design. He has authored and coauthored over 30 referred papers, five issued, and six pending patents. He has served in several conference committees, presented several conference tutorials, served as an IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS Associate Editor, and is actively involved in Semiconductor Research Corporation (SRC) activities.

Mr. Radu is a recipient of one of the 2007 Mahboob Khan Outstanding Mentor Awards.

Andrew Marshall (SM'90) has been with Texas Instruments Incorporated, Dallas, TX, for over 20 years, where he currently works with the Silicon Technology Development Organization. His research interests include the definition of process performance metrics and the development of circuit designs to evaluate and verify performance and power metrics for deep submicrometer technologies, in both bulk silicon and silicon-on-insulator processes. He is the author or coauthor of over 50 papers and conference presentations, including the book *SOI Design: Analog, Memory and Digital Techniques* (Springer, 2002). He is the inventor or coinventor on almost 50 issued patents.

Mr. Marshall is a Fellow of the Institute of Physics, U.K., a member of the IEEE System-on-Chip Conference committee, and secretary of the IEEE Dallas Section.