# Guest Editorial: Special Section on "Autonomous Silicon Validation and Testing of Microprocessors and Microprocessor-Based Systems"

MICROPROCESSORS are unique. They can be programmed to solve any problem that can be solved algorithmically. On the other hand, microprocessor designs are notoriously complex and very challenging to test. This leads to an interesting question: Can a microprocessor be programmed to test itself? This is the central theme of this Special Issue.

A typical microprocessor or embedded processor may incorporate a wide range of design and manufacturing practices from structured application-specific integrated circuit (ASIC) to full custom design, from manual layout, semicustom layout to fully automatic layout. Therefore, for manufactured microprocessors *silicon validation and testing* technology should go hand-in-hand with the design technology and run the entire gamut of available practices and methodologies. With ever increasing transistor counts and frequency of interfaces together with a burgeoning number of failure mechanisms, the tasks of validating and testing microprocessors and microprocessor-based ICs have become more challenging. Customer quality expectations set high goals for defect coverage while the diversity and density of design (either in microprocessors or in embedded processor-based system-on-chip (SoC) architectures) introduce serious structural difficulties in accessing the internal nodes of such complex designs. Lack of internal access, as well as interaction between local signal channels and global routing makes detection difficult because the traditional testing paradigm of divide and conquer is less applicable.

Effective methodologies for silicon validation and testing from the first stages of silicon prototyping through volume production, manufacturing testing, and subsequent field operation can benefit from the uniqueness of locally available microprocessor hardware that is not found in other designs. A processor has exceptional functional access to every other component of a complex design. The processor's unique programmability can be used to support the validation and testing of itself and its surrounding components as it provides a powerful processing engine that can efficiently handle test application and test control algorithms.

This Special Issue presents a collection of recent work in this field of *autonomous and semiautonomous silicon validation and testing* of microprocessors and microprocessor-based systems. Among the papers submitted for this Special Issue, five were selected. They cover several important aspects of the technical area: from first silicon validation and debug to manufacturing and production testing, including both software-based and hardware-based test techniques and design-for-test methods that range from pure functional instruction-based to structural scan-based, tests. The scope of papers extends from embedded uniprocessors to multicore microprocessors.

The first paper, "First silicon functional validation and debug of multicore microprocessors," by T. J. Foster, D. L. Lastor, and P. Singh, describes silicon validation and debug of multiprocessor chips. The major challenges stem from multilevel and distributed memory systems and the communication complexity among cores. The results on an eight-node AMD Opteron processor-based system are provided.

The second paper, "Software-based self-testing with multiple-level abstractions for soft processor cores," by C.-H. Chen, C.-K. Wei, T.-H. Lu, and H.-W. Gao, contributes to the emerging software-based self-testing (SBST) paradigm for embedded processors. It proposes a hybrid methodology for optimized self-test code development utilizing several levels of abstraction for the different components of a pipelined processor.

The third paper, "Satisfiability-based automatic test program generation and design for testability for microprocessors," by L. Lingappan and N. K. Jha also contributes to the area of software-based self-testing. A satisfiability (SAT)-based methodology for automatic generation of self-test programs for microprocessors is described. In the event that SAT-based test generation does not provide high enough fault coverage, DFT modifications at the RT level are employed to improve gate-level fault coverage.

The fourth paper, "Embedded test decompressor to reduce the required channels and vector memory of tester for complex processor circuit," by Y. Han, Y. Hu, X. Li, H. Li and A. Chandra focuses on reduction of tester channels and vector memory for ATE-based testing applied to complex processors. Test pin count and memory reductions are achieved by the presented embedded test patterns' decompressor design.

The fifth paper, "STEAC: A platform for automatic SOC test integration," by C.-Y. Lo, C.-H. Wang, K.-L. Cheng, Huang, C.-W. Wang, S.-M. Wang, and C.-W. Wu provides a comprehensive analysis and supporting tool for the practical challenges of complex microprocessor-based SOC testing. The discussion includes test scheduling, test access mechanism design, and a test wrapper architecture supporting both scan and functional test. Different techniques are integrated in an automatic SOC test flow that has been demonstrated on a fabricated industrial processor-based SOC.

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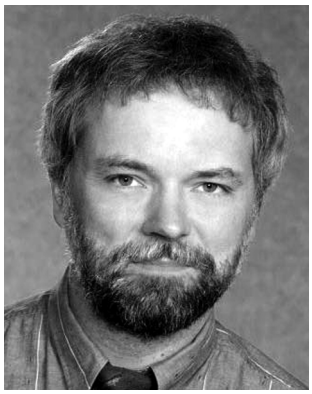

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