

Editorial Appointments for the 2013–2014 Term

I am honored to accept to serve another term as the Editor-in-Chief of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATED (VLSI) SYSTEMS (TVLSI). Previous Editors-in-Chief of this journal have worked tirelessly to bring this journal to the very top. During my previous term the impact factor of TVLSI has moved up from 0.9 to 1.2, which is a significant improvement. I will work with the steering committee and the board to further improve the impact factor of TVLSI. I look forward to the whole community helping with this goal by submitting quality work, accepting reviews, giving valuable comments, and making suggestions. TVLSI had a back log in the acceptance to publication time because of a large number of submissions to the Journal. We have increased the number of pages of TVLSI from 1800 to 2400 and have not accepted any special issues resulting in a significant improvement in this backlog. We will continue this policy and find other ideas to completely eliminate the problem.

I am happy to announce the appointment of Professor Massimo Alioto of NUS as the Associate Editor-in-Chief of TVLSI. Dr. Alioto has a long editorial record and is a well-known scholar in the VLSI area. He will help with TVLSI to further solve any existing issues and further speed up the

review time. In addition, the editorial board was finely tuned by adding associate editors in areas of more submissions and emerging areas. Otherwise, the editorial board remains largely unchanged.

I would like to thank the steering committee of TVLSI for their help with the board formation as well as their valuable advice and directions. I would also like to thank Ms. Mona Mitra, Ms. Michelle Gillespie, Ms. Sonal Parikh, Ms. Rebecca Szewczyk, and other staff members for all their efforts to keep TVLSI running smoothly.

Last, but not the least, I want to express my deep gratitude to the TVLSI Editorial Assistant, Ms. Stacey Weber Jackson, for her steady and extremely efficient service to TVLSI. I am happy that Stacey has agreed to continue working as the Editorial Assistant of TVLSI during my second term.

The biographies and photographs of the Associate Editors on the new editorial board are provided below.

PROF. YEHEA I. ISMAIL, *Editor-in-Chief*
 Director, Center of Nanoelectronics and Devices
 (CND)
 Zewail City of Science and Technology and the
 American University in Cairo
 Cairo, Egypt
 tvlsieic@eecs.northwestern.edu

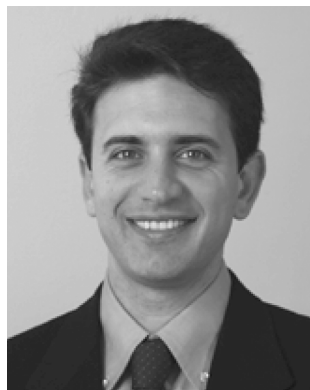
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Yehea Ismail (M'00–SM'10–F'11) received the B.Sc. degree and the M.S. degree from Cairo University, Cairo, Egypt, in 1993 and 1996, respectively, and the M.S. and Ph.D. degrees from the University of Rochester, Rochester, NY, USA, in 1997 and 2000, respectively.

He is the Director of the Nanoelectronics Center, Zewail City, and the American University in Cairo, Cairo, Egypt. He was a tenured Professor with Northwestern University, Evanston, IL, USA, from June 2000 to May 2011. He is the distinguished lecturer of IEEE CASS. He has published over 200 papers in the top refereed journals and conferences and holds many patents. He co-authored three books: *On-Chip Inductance in High Speed Integrated Circuits* (Springer, 2001), *Handbook on Algorithms for VLSI Physical Design* (CRC Press, 2008), and *Temperature-Aware Computer Architecture* (Morgan Kaufmann, 2009). He holds many patents in the area of high performance circuit and interconnect design and modeling. His work is some of the most highly cited in the VLSI area and is extensively used by industry.

Dr. Ismail is the Editor-in-Chief of the IEEE TRANSACTION ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (TVLSI) and the chair elect of the IEEE VLSI Technical Committee. He is on the editorial board of the *Journal of Circuits, Systems, and Computers*, was on the editorial board of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: FUNDAMENTAL THEORY AND APPLICATIONS, and a guest editor for a special issue of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS on “On-Chip Inductance in High Speed Integrated Circuits”. He has also chaired many conferences such as GLSVLSI, IWSOC, ISCAS. He is the Chief Scientist of the Innovation and Entrepreneurship Center of the Ministry of Communications and Information Technology, Egypt. He was a recipient of several awards including the USA National Science Foundation Career Award, the IEEE CAS Outstanding Author Award, Best Teacher Award at Northwestern University, many Best Paper Awards, and Teaching Awards.



Massimo Alioto (M'01–SM'07) was born in Brescia, Italy, in 1972. He received the laurea degree in electronics engineering and the Ph.D. degree in electrical engineering from the University of Catania, Catania, Italy, in 1997 and 2001, respectively.

In 2002, he joined the Dipartimento di Ingegneria dell'Informazione (DII), University of Siena, Siena, Italy, as a Research Associate and in the same year as an Assistant Professor. In 2005, he was appointed Associate Professor of Electronics, and was engaged in the same faculty in 2006. In the summer of 2007, he was a Visiting Professor at EPFL—Lausanne, Switzerland. In 2009–2011, he is Visiting Professor with BWRC—University of California at Berkeley, Berkeley, CA, investigating on ultra-low power circuits and wireless nodes. Since 2001, he has been teaching undergraduate and graduate courses on advanced VLSI digital design, microelectronics, and basic electronics. He has authored or coauthored more than 160 publications on journals (55+, mostly IEEE Transactions) and conference proceedings. Two of them are among the 25 most downloaded TVLSI papers in 2007 (respectively, 10th and 13th). He is coauthor of the book *Model and Design of Bipolar and*

MOS Current-Mode Logic: CML, ECL, and SCL Digital Circuits (Springer, 2005). His primary research interests include the modeling and the optimized design of CMOS high-performance, low-power and ultra low-power digital circuits, arithmetic and cryptographic circuits, interconnect modeling, design/modeling for variability-tolerant and low-leakage VLSI circuits, circuit techniques for emerging technologies. He is the director of the Electronics Lab at University of Siena (site of Arezzo).

Prof. Alioto is a member of the HiPEAC Network of Excellence. He is the Chair of the “VLSI Systems and Applications” Technical Committee of the IEEE Circuits and Systems Society, for which he is also Distinguished Lecturer. He is regularly invited to give talks and tutorials to academic institutions, conferences, and companies throughout the world. He has served as a member of various conference technical program committees (ISCAS, ICCD, PATMOS, ICM, ECCTD, CSIE) and Track Chair (ISCAS, ICCD, ICECS, ICM). He was the Technical Chair of the conference ICM 2010. He serves as Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, as well as of the *Microelectronics Journal*, the *Integration—The VLSI Journal*, the *Journal of Circuits, Systems, and Computers*, the *Journal of Low Power Electronics and Applications*, and the *ACM Transactions on Design Automation of Electronic Systems*. He is Guest Editor of the Special Issue “Advances in Oscillator Analysis and Design” of the *Journal of Circuits, Systems, and Computers* (2010), and Technical Program Chair for the *ICM 2010* Conference.



Paul Ampadu (M'99–SM'11) received the Ph.D. degree from Cornell University, Ithaca, NY, USA, in 2004.

He is an Associate Professor with the Department of Electrical and Computer Engineering (ECE), University of Rochester, Rochester, NY, USA, and the 2011–2013 Dr. Martin Luther King, Jr. Visiting Associate Professor of the Department of Electrical Engineering and Computer Science (EECS), Massachusetts Institute of Technology, Cambridge, MA, USA. From 2001 to 2002 and in the summers of 1999 and 2000, he conducted research at the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, where he investigated energy-efficient VLSI implementation of complex signal processing functions. He and his team have authored three books on error- and temperature-control for networks-on-chip, as well as several dozen scholarly articles in prestigious IEEE/ACM journals and conference proceedings. His research interests include networks-on-chip error control, energy-efficient fault-tolerant circuits for emerging nanoelectronics, low-voltage/low-power VLSI, and efficient design of embedded communication

and signal processing functions.

Dr. Ampadu was a recipient of several international awards, including a Semiconductor Research Corporation (SRC) Master's Scholarship, an IBM Ph.D. Fellowship, a Provost Multidisciplinary Research Award, and many federal grants. He was selected for a NASA Summer Faculty Fellowship, a U.S. Black Engineer of the Year Special Recognition Award, a Charles Drew Professor's Choice Award for mentoring, and the Prestigious NSF CAREER Award. In addition, he and his research team were Best Paper finalists at the 2011 International Symposium on Networks-on-Chip (NOCS). He is an elected member of the IEEE Circuits and Systems Board of Governors and chairs its Ph.D./GoLD subcommittee. He serves on the IEEE Circuits and Systems Technical Committees on VLSI, Nano-Giga, and Circuits and Systems for Communication and has served on the organizing committees of several IEEE and ACM international conferences.



Iris Bahar received the B.S. and M.S. degrees in computer engineering from the University of Illinois, Urbana-Champaign, IL, USA, and the Ph.D. degree in electrical and computer engineering from the University of Colorado, Boulder, CO, USA.

From 1987 to 1992, she worked for Digital Equipment Corporation (in what is now the Intel Hudson facility), and was part of the NVAX Microprocessor Design Team. Since 1996, she has been with the Division of Engineering, Brown University, Providence, RI, USA, where she is currently an Associate Professor. Her research interests include power-aware computer architecture; computer-aided design for synthesis, verification, and low-power applications; and design, test, and reliability issues for nanoscale systems.



Valeriu Beiu (S'92–M'95–SM'96) received the M.Sc. degree in computer engineering from the “Politehnica” University of Bucharest, Bucharest, Romania, in 1980, and the Ph.D. degree with *summa cum laude* in electrical engineering from the Katholieke Universiteit Leuven, Leuven, Belgium, in 1994.

Upon graduation, for two years he has been working on high-speed CPUs and FPUs with the Research Institute for Computer Techniques, Bucharest, Romania, prior to returning to the “Politehnica” University of Bucharest. Since 1991, he has been on leave of absence as follows: Katholieke Universiteit Leuven (1991–1994, Leuven, Belgium), King’s College London (1994–1996, London, U.K.), and Los Alamos National Laboratory (1996–1998, Los Alamos, NM, USA). In 1998, he cofounded RN2R (Dallas, TX, USA) a VLSI IP startup company, and was its Chief Technical Officer (1998–2001). In 2001, he joined the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA, USA, and in 2005 he became Visiting Professor with the School of Computing and Intelligent Systems, University of Ulster,

Ulster, U.K. Since 2006, he has been the Associate Dean for Research and Graduate Studies, Faculty of Information Technology, United Arab Emirates University, Al Ain, Abu Dhabi, UAE. He holds 11 patents, has given over 150 invited talks, and authored over 170 technical papers in journals and conferences. He has authored six chapters (out of which five invited), and is working on one book on emerging brain-inspired nano-architectures, and another one on the VLSI complexity of discrete neural networks. His main research interests include VLSI-efficient designs (low-power and highly reliable) and emerging nano-architectures (massively parallel, fault-tolerant, communication starved, adaptive/reconfigurable), as well as their optimal implementations inspired by neural networks and biological arrays.

Dr. Beiu was a recipient of five fellowships including: Fulbright (1991), Human Capital and Mobility (1994–1996) with King’s College London (“Programmable Neural Arrays” Project), Director’s Funded Postdoc (1996–1998) with Los Alamos National Laboratory (“Field Programmable Neural Arrays” Project, under the Deployable Adaptive Processing Systems initiative), and Fellow of Rose Research (1999–2001). He was the principal investigator (PI) or co-PI of over 60 research contracts totaling over US\$ 22M. He was a recipient of 7 Best Paper Awards. He is a founding member of the European Neural Network Society (ENNS), and a member of: the International Neural Network Society (INNS), the Association for Computing Machinery (ACM), and the Marie Curie Fellowship Association (MCFA). He was a member of the SRC-NNI Working Group on Novel Nano-architectures (2003–2006), of the IEEE CS Task Force on Nanoarchitectures (since 2005), and of the IEEE Emerging Technologies Group on Nanoscale Communications (since 2010). He has organized over 50 conferences/workshops and chaired over 40 conference sessions, was the Program Chairman of the IEEE Los Alamos Section (1997), was an Associate Editor of the IEEE TRANSACTIONS ON NEURAL NETWORKS (2005–2008), and since 2010 is an Associate Editor of the *Nano Communication Networks* (Elsevier).



Sanjukta Bhanja received the Bachelor's degree in electrical engineering from Jadavpur University, Calcutta, in 1991, the Master's degree from Indian Institute of Science, Bangalore, India, in 1994, and the Ph.D. degree in computer science and engineering from the University of South Florida (USF), Tampa, FL, USA, in 2002.

She is currently an Associate Professor with the Department of Electrical Engineering, USF. Her primary research focus is on non-CMOS nano-computing, exploring novel state variables, alternate computing paradigm with heterogeneous devices, VLSI design automation with emphasis on data-driven uncertainties, trade-off of error, power, and reliability at various levels of design abstractions. She has published over 60 publications in top-tier peer-reviewed journal and conferences in VLSI and nano-electronics area.

Dr. Bhanja is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. She has served on the Technical Program Committee of various IEEE and ACM conferences. She is currently the "Emerging Technology track" co-chair in IEEE DATE'11 and has served as Technical Program Co-Chair of IEEE ISVLSI, ACM GLSVLSI and as General Co-Chair of ACM GLSVLSI. She was a recipient of the New Researcher Award from the University of South Florida in 2002, the NSF CAREER Award (2007–2012), USF Tau Beta Pi "Outstanding Engineering Faculty Researcher" Award in 2007, the USF 2008 "Outstanding Faculty Research Achievement Award," the 2010 Florida Education Foundation (F.E.F) William Jones Outstanding Mentor Award, and the USF 09/10 Outstanding Undergraduate Teaching Award.



Chirn Chye Boon (M'09–SM'10) received the B.E. degree (Hons.) in electronics and the Ph.D. degree in electrical engineering from Nanyang Technological University (NTU), Singapore, in 2000 and 2004, respectively.

In 2005, he joined NTU as a Research Fellow and became an Assistant Professor in the same year. Before that, he was with Advanced RFIC, where he worked as a Senior Engineer. He specializes in the areas of radio frequency (RF) and MM-wave circuits and systems design for biomedical and communications applications. He has coauthored over 49 refereed publications and several patents in the fields of RF and MM-wave. He is a coauthor of the book *Design of CMOS RF Integrated Circuits and Systems* (World Scientific Publishing, 2010).

Prof. Boon serves as a committee member for various conferences and is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He is the Programme Director for RF and MM-wave research in the SG\$50 millions research centre of excellence, VIRTUS (NTU) since March 2010. He is the Principal/Co-Principal Investigator for research grants of more than SG\$3,250,000.



Chaitali Chakrabarti received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, and the M.S. and Ph.D. degrees in electrical engineering from the University of Maryland, College Park, MD, USA.

She has been a Professor with Arizona State University (ASU), Tempe, AZ, USA, since 1990. Her research interests include the areas of specialized architectures for signal processing and wireless communications, software defined radio, algorithm-architecture co-design, low power algorithms, and energy-efficient embedded system design including those powered by fuel cells.

Dr. Chakrabarti is a member of the Consortium of Embedded Systems and the Sensor, Signal, and Information Processing Center, ASU. She was a recipient of the Research Initiation Award from the National Science Foundation in 1993, a Best Teacher Award from the College of Engineering and Applied Sciences in 1994, and the Outstanding Educator Award from the IEEE Phoenix section in 2001. She has been on the program committees of ICASSP, ISCAS, SiPS, ASAP, DAC, and ISLPED. She served as an Associate Editor (AE) of the IEEE TRANSACTIONS ON SIGNAL PROCESSING (1999–2005) and also as an Associate Editor of the *Journal of VLSI Signal Processing Systems*. She is the Chair of the Technical Committee of Design and Implementation of Signal Processing Systems, IEEE Signal Processing Society.



Chip-Hong Chang (S'92–M'98–SM'03) received the B.Eng. (Hons.) degree from the National University of Singapore, Singapore, in 1989, and the M.Eng. and Ph.D. degrees from Nanyang Technological University (NTU), Singapore, in 1993 and 1998, respectively.

He served as a Technical Consultant in industry prior to joining the School of Electrical and Electronic Engineering (EEE), NTU, in 1999, where he is currently an Associate Professor. He holds joint appointments with the university as an Assistant Chair of Alumni of the School of Electrical and Electronic Engineering (EEE) since June 2008, the Deputy Director of the Center for High Performance Embedded Systems since 2000, and the Program Director of the Center for Integrated Circuits and Systems from 2003 to 2009. His current research interests include low power arithmetic circuits, residue number system, digital filter design, and digital watermarking for VLSI intellectual property protection. He has coedited one book, published three book chapters, and over 170 research papers in refereed international journals and conferences.

Dr. Chang has served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS in 2010–2011 and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS since 2011, Editorial Advisory Board Member of the *Open Electrical and Electronic Engineering Journal* since 2007 and Editorial Board Member of the *Journal of Electrical and Computer Engineering* since 2008. He also served as a Guest Editor for the special issue of the *Journal of Circuits, Systems, and Computers* in 2010, and in several international conference advisory and technical program committees. He is a Fellow of the IET. He was the corecipient of two paper awards at PrimeAsia 2010 and the finalist of the Best Paper Award at VLSI'95.



Jonathan Chang (SM'06–M'93) received the B.S. degree in electrical engineering from National Taiwan University, Taiwan, in 1990, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1994 and 1998, respectively.

He joined Intel Corporation, Santa Clara, CA, in 1998 and since has been engaged in the design of several high-performance microprocessors with emphasis in large, high-speed, low power cache design. He was a Principal Engineer in the area of cache design in Enterprise Microprocessor Group. He joined TSMC, Hsin-Chu, Taiwan, in 2010 as a deputy director and is responsible for high speed embedded SRAM products. He is currently among the technical committee of 2011 VLSI symposium on circuits. He has published over 20 technical papers in IEEE conferences or journals.



Robert Chen-Hao Chang (S'91–M'95–SM'09) received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1987 and 1989, respectively, and the Ph.D. degree in electrical engineering from University of Southern California (USC), Los Angeles, CA, USA, in 1995.

In 1996, he joined the faculty of the Department of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan, where he is currently a Professor. He served as the Director of Meng Yao Chip Center from 2000 to 2004, the Director of Center for Research and Development of Engineering Technology of the College of Engineering from 2005 to 2006, and Chairman of the Electrical Engineering Department from 2006 to 2008. He has published over 90 technical journal and conference papers. His research interests include mixed-signal IC design, power management IC design, low-power circuits design, and baseband circuits design.

Dr. Chang was a recipient of the National Science Council Research Award in 1997 and 1998, the Distinguished Teaching Award, the Outstanding Research Project Award, and the Distinguished Teacher Evaluation Award from National Chung Hsing University in 2004, 2006, and 2009, respectively. He was listed in the Marquis Who's Who in the World 2000. He is a member of Tau Beta Pi. He has been a Member of VLSI Systems and Applications Technical Committee, IEEE Circuits and Systems Society since 2004. He is an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and the Chair of IEEE CASS Taipei Chapter. He also served as Technical Program Committee Member for many conferences.



Deming Chen received the B.S. degree in computer science from University of Pittsburgh, Pittsburgh, PA, USA, in 1995, and the M.S. and Ph.D. degrees in computer science from University of California at Los Angeles, Los Angeles, CA, USA, in 2001 and 2005, respectively.

He worked as a Software Engineer between 1995–1999 and 2001–2002. He has been an Assistant Professor with the Electrical and Computer Engineering Department, University of Illinois, Urbana-Champaign, IL, USA, since 2005. He is a Research Assistant Professor with the Coordinated Science Laboratory and an affiliate Assistant Professor with the Computer Science Department. His current research interests include high-level synthesis, nano-systems design and nano-centric CAD techniques, FPGA synthesis and physical design, microarchitecture and SoC design under parameter variation, and reconfigurable computing.

Dr. Chen is a technical committee member for a series of conferences and symposia, including FPGA, ASPDAC, ICCD, ISQED, DAC, ICCAD, and DATE, etc. He also served as session chair, panelist, panel organizer, or moderator for some of these and other conferences. He is the TPC subcommittee chair for ASPDAC'09–2011 and the CAD Track co-chair for ISVLSI'09 and ISCAS'10–2011. He is the program chair for SLIP'11. He is an Associated Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (TVLSI), IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS (TCAS-I), *Journal of Circuits, Systems and Computers* (JCSC), and *Journal of Low Power Electronics* (JOLPE). He was a recipient of the Achievement Award for Excellent Teamwork from Aplus Design Technologies in 2001, the Arnold O. Beckman Research Award from UIUC in 2007, the NSF CAREER Award in 2008, the ASPDAC'09 Best Paper Award, and the SASP'09 Best Paper Award. He is included in the List of Teachers Ranked as Excellent in 2008. He received the ACM SIGDA Outstanding New Faculty Award in 2010.



Poki Chen (M'05) was born in Chia-Yi, Taiwan, in 1963. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 1985, 1987, and 2001, respectively.

During 1998–2001 and 2001–2006, he was a Lecturer and an Assistant Professor correspondingly with the Electronic Engineering Department, National Taiwan University of Science and Technology (NTUST), Taiwan. He is currently an Associate Professor with the same department. Since 2010, he was selected as the director of System-on-Chip Research Center, NTUST. His research interests include analog/mixed-signal integrated circuits and systems with a special interest focused on time-domain signal processing circuits, such as time-domain smart temperature sensor, time-to-digital converter, digital pulse generator, digital pulse width modulator, and duty cycle corrector. He is also interested in creating innovative analog applications for FPGA platforms, such as FPGA smart temperature sensor, FPGA digital-to-time, and time-to-digital converters.



Pasquale Corsonello was born in Cosenza, Italy, on May 4, 1964. He received the Master's degree in electronics engineering from the University of Naples "Federico II", Naples, Italy, in 1988.

He joined the Institute of Research on Parallel Computers, National Council of Research of Italy, Naples, Italy, where he was working on the design and modelling of electronic transducers for high precision measurement, receiving a post-graduate two-years grant. In 1992, he joined the Department of Electronics, Computer Science, and Systems, University of Calabria, Rende, Italy, as a Research Associate. In 1997, he was appointed an Assistant Professor of electronics with the Department of Electronics Engineering and Applied Mathematics, University of Reggio Calabria, Reggio Calabria, Italy, where he also served as the Director of the Microelectronics Laboratory. In 2001, he was appointed an Associate Professor of electronics and Chair of the Ph.D. Program in electronics engineering at the University of Reggio Calabria. In the summer 2004, he was a Visiting Researcher with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY, USA. In 2005, he was appointed as Adjunct Associate Professor with

the same Department. He is currently an Associate Professor of electronics with the Department of Electronics, Computer Science, and Systems of the University of Calabria, Rende, Italy. His main research interests include high-performance arithmetic circuits, low-power design, VLSI architecture for image processing and multimedia, reconfigurable systems. He has coauthored over 120 technical papers and holds two patents in these fields. One of these papers is among the 25 most downloaded TVLSI papers in 2007.

Prof. Corsonello was a recipient of the Best Paper Award at the 2010 IEEE Conference on Advances in Circuits, Electronics and Micro-Electronics, CENICS 2010. He has also received several grants from both private industries and government agencies for projects in these areas. He serves on technical committees of several VLSI conferences and as a peer reviewer for several VLSI journals. He is an Associate Editor of the *Journal of Low Power Electronics and Applications*.



Vivek De (F'11) received the Bachelor's degree from the Indian Institute of Technology, Madras, India, the Master's degree from Duke University, Durham, NC, USA, and the Ph.D. degree from Rensselaer Polytechnic Institute, Rensselaer, NY, USA, all in electrical engineering.

He is an Intel Fellow and Director of Circuit Technology Research with Intel Labs, Hillsboro, OR, USA. He joined Intel in 1996 as a Staff Engineer in Intel's Circuits Research Lab (CRL). Since that time, he has led research teams in CRL focused on developing advanced circuits and design techniques for low-power and high-performance processors. In his current role as Director of CRL, he is responsible for providing strategic directions for research in future circuit technologies and aligning Intel's circuit research with technology scaling challenges. He has 193 publications in refereed international conferences and journals, and 172 patents, with 31 more patents filed (pending).

Dr. De was a recipient of an Intel Achievement Award for his contributions to a novel integrated voltage regulator technology.



Robert Dick (S'95–M'02) received the B.S. degree from Clarkson University, Potsdam, NY, USA, in 1996, and the Ph.D. degree from Princeton University, Princeton, NJ, in 2002.

He is an Associate Professor with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor. He worked as a Visiting Professor with the Department of Electronic Engineering, Tsinghua University, in 2002, as a Visiting Researcher at NEC Labs America in 1999, and was on the faculty of Northwestern University from 2003 to 2008. He has published in the areas of embedded operating systems, data compression, embedded system synthesis, dynamic power management, low-power and temperature-aware integrated circuit design, wireless sensor networks, human perception aware computer design, reliability, embedded system security, and behavioral synthesis.

Prof. Dick was a recipient of an NSF CAREER Award and won his department's Best Teacher of the Year Award in 2004. In 2007, his technology won a Computerworld Horizon Award and his paper was selected as one of the 30 in a collection of high-impact DATE papers appearing during the past 10 years. His 2010 work won a Best Paper Award at DATE. He is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, a Guest Editor for *ACM Transactions on Embedded Computing Systems*, was selected as Technical Program Committee Co-Chair of the 2011 International Conference on Hardware/Software Codesign and System Synthesis, and serves on the technical program committees of several embedded systems and CAD/VLSI Conferences.



Nikil D. Dutt (F'08) received the Ph.D. degree in computer science from the University of Illinois at Urbana-Champaign, Urbana-Champaign, IL, USA, in 1989.

He is currently a Chancellor's Professor with the University of California, Irvine, with academic appointments in the Computer Science and Electrical Engineering and Computer Science Departments. His research interests include embedded systems design automation, computer architecture, optimizing compilers, system specification techniques, and distributed embedded systems.

Dr. Dutt was a recipient of Best Paper Awards at CHDL89, CHDL91, VLSIDesign2003, CODES+ISSS 2003, CNCC 2006, and ASPDAC-2006. He was an ACM SIGDA Distinguished Lecturer during 2001–2002, and an IEEE Computer Society Distinguished Visitor for 2003–2005. He has served on the steering, organizing, and program committees of several premier CAD and Embedded System Design conferences and workshops, including ASPDAC, CASES, CODES+ISSS, DATE, ICCAD, ISLPED, LCTES, RTAS, and RTSS. He serves or has served on the advisory boards of ACM SIGBED and ACM SIGDA and is Vice-Chair of IFIP WG 10.5.



Ibrahim (Abe) Elfadel received the Ph.D. degree from Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 1993.

He is a Professor of Microsystems Engineering with the Masdar Institute of Science and Technology, Abu Dhabi, UAE, where he is a lead principal investigator in TwinLab/3DSCI, a joint collaborative research center on 3-D integrated circuits between the Technical University of Dresden, Germany, and the Masdar Institute of Science and Technology. Between 1996 and 2010, he was with the corporate CAD organizations at IBM Research and the IBM Systems and Technology Group, Yorktown Heights, NY, USA, where he was involved in the research, development, and deployment of CAD tools and methodologies for IBM's high-end microprocessors. Between 2000 and 2004, he was an adjunct Associate Professor of electrical engineering with Columbia University, New York City, NY, USA. In addition to 3-D integrated circuits, his current research interests include power and thermal management of multi-core processors; variation-aware, low-power digital systems design; embedded, low-power digital-signal processing; and modeling and integration

of micro power sources.

Dr. Elfadel was a recipient of six Invention Achievement Awards, one Outstanding Technical Achievement Award, and one Research Division Award, all from IBM, for his contributions in the area of VLSI CAD. He is inventor or co-inventor on more than 50 issued and pending patents. He is currently serving as an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS.



Maged Ghoneima (M'97) received the B.Sc. degree in electronics and communications engineering with Honors and the M.Sc. degree in electronics from Ain Shams University, Cairo, Egypt, in 1997 and 2000, and the Ph.D. degree in computer engineering from Northwestern University, Evanston, IL, USA, in 2006.

In 1997, he was appointed as a Teacher Assistant with the Department of Electrical and Computer Engineering, Ain Shams University. In 2002, he was with OEA International and with the Circuit Research Lab, Intel Corporation, from 2003 to 2005. He is currently a Senior Circuit Design Engineer with the VLSI Circuit Design Group, NVIDIA Corporation, Santa Clara, CA, since 2006 developing on-chip memory structures for the Tesla and Fermi GPUs. He has authored and coauthored over 25 technical papers in refereed international conferences and journals. He also holds two patents and more than five filed in the area of low-power and high performance circuit design. His research interests include on-chip interconnect architectures, on-chip memory structures, low power circuit design, and related circuit level issues in high performance VLSI circuits.

Dr. Ghoneima was a recipient of the Walter Murphy and Capbell Fellowship Awards from Northwestern University in 2001 and 2005, in addition to the Intel Ph.D. Fellowship Award in 2004.



Patrick Girard (SM'09) received the M.S. degree in electrical engineering and the Ph.D. degree in microelectronics from the University of Montpellier, Montpellier, France, in 1988 and 1992, respectively.

He is currently Research Director with French National Center for Scientific Research (CNRS), and Head of the Microelectronics Department, Laboratory of Informatics, Robotics and Microelectronics of Montpellier—France (LIRMM). His research interests include all aspects of digital testing and memory testing, with emphasis on critical constraints such as timing and power. He is a co-editor of the book *Power-Aware Testing and Test Strategies for Low Power Devices* (Springer, 2009) and a coauthor of the book *Advanced Test Methods for SRAMs—Effective Solutions for Dynamic Fault Detection in Nanoscale Technologies* (Springer, 2009). He has supervised 26 Ph.D. dissertations and has published 6 books or book chapters, 36 journal papers, and more than 130 conference and symposium papers on these fields.

Dr. Girard was Vice-Chair of the European Test Technology Technical Council (ETTTTC) of the IEEE Computer Society from 2006 to 2010. He has served on numerous conference committees including ACM/IEEE Design Automation Conference (DAC), ACM/IEEE Design Automation and Test in Europe (DATE), IEEE International Test Conference (ITC), IEEE International Conference on Computer Design (ICCD), IEEE VLSI Test Symposium (VTS), IEEE European Test Symposium (ETS), IEEE Asian Test Symposium (ATS), and ACM/IEEE International Symposium on Low Power Electronic Design (ISLPED). He is the founder and Editor-in-Chief of the *ASP Journal of Low Power Electronics* (JOLPE). He is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and the *Journal of Electronic Testing—Theory and Applications* (JETTA—Springer). From 2005 to 2009, he was an Associate Editor of the IEEE TRANSACTIONS ON COMPUTERS. He has been involved in several European research projects (ESPRIT III ATSEC, EUREKA MEDEA, MEDEA+ ASSOCIATE, IST MARLOW, MEDEA+ NanoTEST, CATRENE TOETS) and has managed industrial research contracts with major companies like Infineon Technologies, Intel, Atmel, STMicroelectronics, etc. He was a recipient of two Best Paper Awards (ETS 2004 and DDECS 2005).



Dimitris Gizopoulos (SM'03) received the engineering diploma from the Computer Engineering and Informatics Department, University of Patras, Patras, Greece, in 1992, and the Ph.D. degree from the Department of Informatics and Telecommunications, University of Athens, Panepistimiopolis, Greece, in 1997.

He is an Associate Professor with the Department of Informatics and Telecommunications, University of Athens, Panepistimiopolis, Greece. He was previously leading the Computer Systems Laboratory, Department of Informatics, University of Piraeus, Greece. His research interests include dependable computer architecture, microprocessors and microprocessor-based systems self-testing, online testing, and fault tolerance, as well as embedded and real-time systems design. He has published over 100 papers in peer reviewed transactions, journals, and conference proceedings, and is an inventor of a U.S. patent, author of a book, and editor of a second.

Dr. Gizopoulos is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, the IEEE TRANSACTIONS ON COMPUTERS, the *IEEE Design and Test of Computers Magazine*, and *Springer's Journal of Electronic Testing: Theory and Applications*, as well as guest editor for several special issues. He was member of the Steering Committees of the IEEE International Test Conference and IEEE European Test Symposium. He served as general chair and/or program chair of the IEEE European Test Symposium, the IEEE International On-Line Testing Symposium, and the IEEE International Symposium on Defect and Fault Tolerance. He serves on the Organizing and Program Committees of several international IEEE and ACM conferences and he is member of the Executive Committee of the IEEE Computer Society Test Technology Technical Council (TTTC). He is a Golden Core Member of IEEE Computer Society and a member of ACM and SIGARCH.



Yajun Ha (S'98–M'04–S'09) received the B.S. degree from Zhejiang University, China, in 1996, the M.Eng. degree from National University of Singapore, Singapore, in 1999, and the Ph.D. degree from Katholieke Universiteit Leuven (KULeuven), Leuven, Belgium, in 2004, all in electrical engineering.

From January 1999 to February 2004, he worked as a researcher with the Inter-University MicroElectronics Center (IMEC), Leuven, Belgium. Since February 2004, he has been with the Department of Electrical and Computer Engineering, National University of Singapore, where he is currently an Assistant Professor. His research interests include the general area of embedded computing (VLSI) architecture and design methodologies, with the focus on reconfigurable computing. He has published around 60 internationally peer-reviewed journal/conference papers on these topics.

Dr. Ha has served a number of positions in the professional communities. He serves as the Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS (2011–2013), the Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (2013–2014), and the *Journal of Low Power Electronics* (since 2009). He serves as the General Co-Chair of ASP-DAC 2014; Program Co-Chair for FPT 2010; Chair of the Singapore Chapter of the IEEE Circuits and Systems (CAS) Society (2011 and 2012); Member of ASP-DAC Steering Committee; and Member of IEEE CAS VLSI and Applications Technical Committee. He is the Program Committee Member for a number of well-known conferences in the fields of embedded systems and FPGAs, such as DATE, ASP-DAC, FPL, FPT.



Pavan Kumar Hanumolu received the B.E. (Hons.) degree from the Birla Institute of Technology and Science, Pilani, India, in 1998, the M.S. degree from the Worcester Polytechnic Institute, Worcester, MA, USA, in 2001, and the Ph.D. degree from the Oregon State University, Corvallis, OR, USA, in 2006.

He is currently an Assistant Professor with the School of Electrical Engineering and Computer Science, Oregon State University. His research interests include high-speed, low-power I/O interfaces, digital techniques to compensate for analog circuit imperfections, time-based data converter techniques, and power-management circuits.

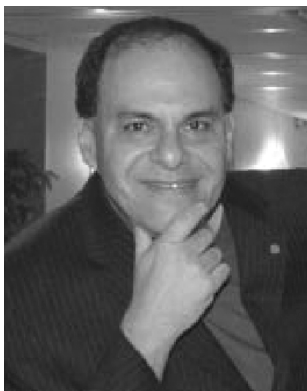
Dr. Hanumolu was a recipient of the National Science Foundation CAREER Award in 2010, the Engelbrecht Young Faculty Award in 2009, and the Professor of the Year Award in 2008 from the College of Engineering and the School of EECS, Oregon State University, respectively. He was a corecipient of the Custom Integrated Circuits Conference (CICC) 2006 Best Student Paper Award. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II:

EXPRESS BRIEFS from 2008 to 2010 and the Guest Editor of the *IEEE Journal of Solid-State Circuits*. He currently serves as a member of the IEEE Custom Integrated Circuits Conference Technical Program Committee and Analog Signal Processing Program Committee of the IEEE International Symposium on Circuits and Systems.



Mona Mostafa Hella (SM'96–M'01) received the B.Sc. and Master's degrees with Honors from Ain-Shams University, Cairo, Egypt, in 1993 and 1996, and the Ph.D. degree from The Ohio-State University, Columbus, OH, USA, in 2001, all in electrical engineering.

From 1993 to 1997, she was a Teaching and Research Assistant with Ain-Shams University. From 1997 to 2001, she was a Research Assistant with the Ohio State University. She was with the Helsinki University of Technology (HUT), Espoo, Finland, as a Visiting Scholar in the summer of 1998, and with the Analog Group, Intel Corporation, Chandler, AZ, USA, in Summer 1999. She was a Senior Designer at Spirea AB, Stockholm, Sweden, working on CMOS power amplifiers (2000–2001). From 2001 to 2003, she was a Senior Designer at RFMD Inc, Billerica, MA, USA, working on Optical communication systems, as well as silicon-based wireless systems. She joined the Electrical, Computer, and Systems Engineering Department, Rensselaer Polytechnic Institute as an Assistant Professor in 2004. Her research interests include the areas of mixed-signal and RFIC design for wireless and wireline applications.



Mohammed Ismail (F'08) is a Professor and Founding Director of the Analog VLSI Lab, The Ohio State University, Corvallis, OH, USA, and of the RaMSiS Group, KTH, Stockholm, Sweden. He is also affiliated with the ElectroScience Lab, Ohio State University. Currently, he conducts research on robust low power RF and MM-wave ICs for wireless, bio, and multimedia applications with a focus on manufacturable low cost high volume CMOS solutions for mobile and wearable embedded devices. He served as a Corporate Consultant to over 30 companies and is a Co-Founder of Firstpass Technologies, Inc., a developer of RF and mixed signal IPs. He co-founded ANACAD-Egypt (now part of Mentor Graphics). He advised the work of 50 Ph.D. students and over 100 M.S. students. He authored or coauthored a dozen books and over 250 journal publications. He is the Founding Editor-in-Chief of the *Journal of Analog Integrated Circuits and Signal Processing* (Springer) and the Founder of the IEEE ICECS, the flagship Region 8 conference of the IEEE Circuits and Systems Society.

Dr. Ismail was a recipient of the U.S. Presidential Young Investigator Award, the Ohio State Lumley Research Award four times, in 1992, 1997, 2002, and 2007, and the U.S. Semiconductor Research Corporation's Inventor Recognition Award twice. He has served the IEEE in many editorial and administrative capacities.



Dr. Rajiv V. Joshi (F'02) received the B.Tech. degree from Indian Institute of Technology, Bombay, India, the M.S. degree from Massachusetts Institute of Technology, Boston, MA, USA, and the Doctorate in engineering science from Columbia University, New York, NY, USA.

He is a Research Staff Member with T. J. Watson Research Center, IBM, Yorktown Heights, NY, USA. He developed novel interconnect processes and structures for Aluminum, tungsten and Copper technologies which are widely used in IBM for various sub-0.5 μm memory and logic technologies as well as across the globe. His circuit related work includes design of register files, registers, latches, L1, L2 Caches, TLB, IO circuits development of physical design tools, and CAD-based library generation and circuit designs in SOI technology. His recent work related to 8T stable 6 GHz SRAM cell was covered by EE times. He contributed through IP and designs to IBM PowerPC program taking leadership role in SRAM technology, cell analysis/modeling and stability enhancement. He led successfully the Technology driven SRAM at IBM Server Group. He is a master inventor and key technical leader with IBM research division. He has authored and coauthored over 160 research papers and presented several invited and keynote talks. He holds 155 U.S. patents in addition to several pending patents.

Dr. Joshi was a recipient of an Outstanding Technical Achievement Award for his contributions to IBM microprocessor designs. He has won 50 invention plateau achievement awards from IBM and won two divisional patent portfolio awards for cross-licensing and utilization of his patents in the IBM products. He received three *Corporate Patent Portfolio Awards* from IBM for licensing contributions. He received the Lewis Winner Award in 1992 for an outstanding paper he coauthored at the International Solid State Circuit Conference. He was instrumental in starting interconnect workshop in early 1980s. He chaired advanced interconnect conferences sponsored by MRS and served as an editor of the proceedings. He is a fellow of ISQED and serves as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He served on committees of ISLPED (International Symposium Low Power Electronic Design) IEEE VLSI Design, IEEE International SOI Conference ISQED Program committees.

Dr. Joshi was a recipient of an Outstanding Technical Achievement Award for his contributions to IBM microprocessor designs. He has won 50 invention plateau achievement awards from IBM and won two divisional patent portfolio awards for cross-licensing and utilization of his patents in the IBM products. He received three *Corporate Patent Portfolio Awards* from IBM for licensing contributions. He received the Lewis Winner Award in 1992 for an outstanding paper he coauthored at the International Solid State Circuit Conference. He was instrumental in starting interconnect workshop in early 1980s. He chaired advanced interconnect conferences sponsored by MRS and served as an editor of the proceedings. He is a fellow of ISQED and serves as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He served on committees of ISLPED (International Symposium Low Power Electronic Design) IEEE VLSI Design, IEEE International SOI Conference ISQED Program committees.



Tanay Karnik (M'88–SM'04) received the Ph.D. degree in computer engineering from the University of Illinois at Urbana-Champaign, Urbana-Champaign, IL, USA, in 1995.

He is a Principal Engineer and Program Director with the Academic Research Office, Intel Laboratories, Hillsboro, OR, USA. His research interests include the areas of variation tolerance, power delivery, soft errors, and physical design. He has published over 45 technical papers, has 44 issued and 33 pending patents in these areas.

Dr. Karnik was a recipient of an Intel Achievement Award for the pioneering work on integrated power delivery. He has presented several invited talks and tutorials, and has served on five Ph.D. students' committees. He was a member of ISSCC, DAC, ICCAD, ICICDT, and ISQED program committees and JSSC, TCAD, TVLSI, and TCAS review committees. He was the General Chair of ASQED'10, ISQED'08, ISQED'09, and ICICDT'08. He is an ISQED Fellow and a Guest Editor for the IEEE JOURNAL ON SOLID-STATE CIRCUITS and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.



Chulwoo Kim (S'98–M'02–SM'06) received the B.S. and M.S. degrees in electronics engineering from the Korea University, Seoul, South Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Urbana-Champaign, IL, USA, in 2001.

In 1999, he worked as a summer intern with Design Technology, Intel Corporation, Santa Clara, CA, USA. In May 2001, he joined IBM Microelectronics Division, Austin, TX, USA, where he was involved in cell processor design. Prior to joining IBM, he was a Research Staff Member with the University of California, Santa Cruz, CA, USA, in 2001. Since September 2002, he has been with the Department of Electronics Engineering, Korea University, where he is currently an Associate Professor. In 2008–2009, he was a Visiting Scholar with the University of California, Los Angeles, Los Angeles, CA, USA. His current research interests include the areas of wireline transceiver, memory, power management, and data converters.

Dr. Kim was a recipient of the Samsung HumanTech Thesis Contest Bronze Award (1996), the ISLPED Low-Power Design Contest Award (2001), the DAC Student Design Contest Award (2002), SRC Inventor Recognition Awards (2002), the Young Scientist Award from the Ministry of Science and Technology of Korea (2003), the Seoktop Award for excellence in teaching (2006) and 13th ASP-DAC Best Design Award (2008). He is currently on the editorial board of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.



Ram K. Krishnamurthy (F'11) received the B.E. degree in electrical engineering from Regional Engineering College, Trichy, India, in 1993, and the Ph.D. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 1998.

He is a Senior Principal Engineer with Circuits Research Laboratory, Intel Labs, Hillsboro, OR, USA, where he heads the high-performance and low-voltage circuits research group. He has been with Intel Corporation since 1998. He holds 84 issued patents with 90 patents pending and has published over 100 conference/journal papers and 3 book chapters on high-performance energy-efficient microprocessor design.

Dr. Krishnamurthy was a recipient of two Intel Achievement Awards, in 2004 and 2008, for the development and technology transfer of novel high-performance execution core arithmetic circuits and special-purpose hardware encryption accelerators. He serves as Intel's representative on the SRC Integrated Circuits and Systems Sciences Task Force, has been a guest editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and on the technical program committees of the ISSCC, CICC, and SOCC conferences. He served as the Technical Program Chair/General Chair for the 2005/2006 IEEE International Systems-on-Chip Conference and presently serves on the conference's steering committee.



Nasser A. Kurd received the M.S.E.E. degree from University of Texas in San Antonio (UTSA), San Antonio, TX, USA, in 1995.

He joined Intel Corporation, Hillsboro, OR, USA, in 1996, where he is currently a Senior Principal Engineer with the Microprocessor Development Circuit Technology Group leading next generation microprocessor clocking technologies. He has been involved in clocking, analog design, analog process scaling, and I/O for several microprocessor generations. Between 1994–1996, he was with AMD, Austin, TX, USA, in the 29K Microprocessor Development Group.

Mr. Kurd has served on several conference committees, authored and coauthored several internal and external publications, and holds 29 granted patents.



Volkan Kursun received the B.S. degree in electrical and electronics engineering from the Middle East Technical University, Ankara, Turkey, in 1999, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Rochester, Rochester, NY, USA, in 2001 and 2004, respectively.

He performed research on mixed-signal thermal inkjet integrated circuits with Xerox Corporation, Webster, NY, USA, in 2000. During summers 2001 and 2002, he was with Intel Microprocessor Research Laboratories, Hillsboro, OR, USA, where he was responsible for the modeling and design of high frequency monolithic power supplies. During summer 2008, he was a Visiting Professor with the Chuo University, Tokyo, Japan. He served as an Assistant Professor with the Department of Electrical and Computer Engineering, University of Wisconsin, Madison, WI, USA, from August 2004 to August 2008. He has been an Assistant Professor with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, China, since August 2008. His current research interests include the areas of nanoelectronics, low power

and robust integrated circuit design, and gigascale 3-D system-on-chip integration with nanoscale devices and interconnect. He has over 100 publications and six issued and two pending patents in the areas of high performance integrated circuits and novel semiconductor devices. He is the author of the book *Multi-Voltage CMOS Circuit Design* (Wiley, 2006).

Dr. Kursun served on the editorial boards of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS from 2007 to 2010 and 2005 to 2008, respectively. He is a member of the technical program and organizing committees of a number of IEEE and ACM conferences and currently serves on the editorial boards of the *Journal of Circuits, Systems, and Computers (JCSC)*, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and the *Journal of Low Power Electronics and Applications (JLPEA)*.



Mohammad M. Mansour (S'10) received the B.E. degree with distinction and the M.E. degree from the American University of Beirut (AUB), Beirut, Lebanon, in 1996 and 1998, respectively, both in computer and communications engineering, and the M.S. degree in mathematics and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign (UIUC), Urbana, IL, USA, in 2002 and 2003, respectively.

He is currently an Associate Professor of electrical and computer engineering with the Electrical and Computer Engineering Department, AUB, Beirut, Lebanon. From December 2006 to August 2008, he was on research leave with QUALCOMM Flarion Technologies, Bridgewater, NJ, where he worked on modem design and implementation for 3GPP-LTE, 3GPP-UMB, and peer-to-peer wireless networking PHY layer standards. From 1998 to 2003, he was a Research Assistant with the Coordinated Science Laboratory (CSL), UIUC. He joined the faculty at AUB in Fall 2003. During the summer of 2000, he worked at National Semiconductor Corporation, San Francisco, CA, USA, with the Wireless Research Group. In 1997, he was a Research Assistant with the Electrical and

Computer Engineering Department, AUB, and in 1996, he was a Teaching Assistant with the same department. His research interests include VLSI design and implementation for embedded signal processing and wireless communications systems, coding theory and its applications, digital signal processing systems, and general purpose computing systems.

Prof. Mansour is a member of the Design and Implementation of Signal Processing Systems Technical Committee of the IEEE Signal Processing Society. He has been serving as an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS since April 2008, Associate Editor for *ISRN Applied Mathematics* since December 2010, and Associate Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS since December 2010. He is the technical co-chair of the IEEE SIPS 2010 workshop. He was the recipient of the PHI Kappa PHI Honor Society Award twice in 2000 and 2001, and the Hewlett Foundation Fellowship Award in March 2006.



Malgorzata Marek-Sadowska received the M.S. degree in applied mathematics and the Ph.D. degree in electrical engineering from Politechnika Warszawska (Technical University of Warsaw), Warsaw, Poland.

From 1976 to 1982, she was an Assistant Professor with the Institute of Electron Technology, Technical University of Warsaw. She became a Research Engineer with the Electronics Research Laboratory, University of California at Berkeley, Berkeley, in 1982 and continued there until 1990, when she joined the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA, USA, as a Professor.

From 1993 to 1995, Dr. Marek-Sadowska was Editor-In-Chief of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS.



Yehia Massoud (M'99) received the B.Sc. and M.Sc. degrees (with honors) from Cairo University, Cairo, Egypt, and the Ph.D. degree in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 1999.

In July 2003, he joined Rice University, Houston, TX, USA, where he is the founding director of the Rice Automated Nanoscale Design Group (RAND) and an Associate Professor with the Electrical and Computer Engineering, Computer Science, and Applied Physics Departments. He was a member of the Technical Staff with the Advanced Technology Group, Synopsys Inc., Mountain View, CA, USA, from 1999 to 2003. He is also the theme leader for Novel Interconnects and Architectures in the Southwest Academy of Nanoelectronics (SWAN), which is funded by the SRC Nanoelectronics Research Initiative. He leads research efforts targeting the modeling and design of innovative circuits, systems, and interconnect based on both carbon nanotubes and nanophotonic structures. He leads parallel research efforts targeting variability-aware optimization, modeling, and automated synthesis techniques for analog/RF/mixed signal circuits and systems as well as

methodologies for interconnect-centric network-on-chip and thermally-aware design. He has published more than 150 papers in peer reviewed journal and conferences.

Dr. Massoud was a recipient of the Synopsys Special Recognition Engineering Award, the National Science Foundation CAREER Award for 2004, several Best Paper Award nominations, and the Best Paper Award at the 2007 IEEE International Symposium on Quality Electronic Design. He currently serves as the General Co-Chair of the 2009 ACM Great Lakes Symposium on VLSI (GLSVLSI). He is also an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS. He also serves on the Editorial board of the *Journal of Circuits, Systems, and Computers*. He has served as the Technical Program Co-chair of the 2007 ACM Great Lakes Symposium on VLSI. He has chaired or cochaired conference tracks in several IEEE/ACM international conferences, such as the design automation track in ISCAS 2007, ISCAS 2008, ISCAS 2009, the VLSI Design track in GLSVLSI 2006, and the emerging technologies track in ISVLSI 2009. He has also served on the technical program committees of many of the key conferences in Electronic Design Automation, VLSI, and Nanotechnology, such as ICCAD, ISCAS, DATE, and ISQED.



Pramod Kumar Meher (SM'03) received the B.Sc. and M.Sc. degrees in physics and Ph.D. degree in science from Sambalpur University, Sambalpur, India, in 1976, 1978, and 1996, respectively.

He has a wide scientific and technical background covering Physics, Electronics, and Computer Engineering. Currently, he is a Senior Scientist with the Institute for Infocomm Research, Singapore. Prior to this assignment he was a visiting faculty with the School of Computer Engineering, Nanyang Technological University, Singapore. Previously, he was a Professor of Computer Applications with Utkal University, Bhubaneswar, India, from 1997 to 2002, a Reader in Electronics with Berhampur University, Berhampur, India, from 1993 to 1997, and a Lecturer in Physics with various Government Colleges in India from 1981 to 1993. His research interests include design of dedicated and reconfigurable architectures for computation-intensive algorithms pertaining to signal processing, image processing, communication, bio-informatics, and intelligent computing. He has published over 150 technical papers in various reputed journals and conference proceedings.

Dr. Meher is a Fellow of the Institution of Electronics and Telecommunication Engineers, India, and a Fellow of the Institution of Engineering and Technology, U.K. He is serving as a speaker for the Distinguished Lecturer Program (DLP) of the IEEE Circuits and Systems Society, and an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and the *Journal of Circuits, Systems, and Signal Processing*. He was the recipient of the Samanta Chandrasekhar Award for excellence in research in engineering and technology for the year 1999.



Chris J. Myers received the B.S. degree in electrical engineering and Chinese history from the California Institute of Technology, Pasadena, CA, USA, in 1991, and the M.S.E.E. and Ph.D. degrees from Stanford University, Stanford, CA, USA, in 1993 and 1995, respectively.

He is a Professor with the Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT, USA. He is the author of over 100 technical papers and the textbooks *Asynchronous Circuit Design* (Wiley, 2001) and *Engineering Genetic Circuits* (Chapman & Hall/CRC Press, 2009). He is also a co-inventor on four patents. His research interests include asynchronous circuit design, formal verification of analog/mixed signal circuits and cyber-physical systems, and modeling, analysis, and design of genetic circuits.

Dr. Myers was a recipient of an NSF Fellowship in 1991, an NSF CAREER Award in 1996, and Best Paper Awards at Async 1999 and Async 2007.



Seda Ogrenci Memik received the B.S. degree in electrical and electronic engineering from Boğaziçi University, Istanbul, Turkey, and the Ph.D. degree in computer science from University of California, Los Angeles, CA, USA.

She is currently an Associate Professor with the Electrical Engineering and Computer Science Department, Northwestern University, Evanston, IL, USA. Her research interests include embedded and reconfigurable computing, thermal-aware design automation, and thermal management for microprocessor systems.

Prof. Ogrenci Memik was a recipient of the National Science Foundation Early Career Development (CAREER) Award in 2006. She has served as technical program committee member, organizing committee member, and track chair of several conferences, including ICCAD, DATE, FPL, GLSVLSI, and ISVLSI and she is currently serving on the Editorial Board of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.



Sule Ozev received the Ph.D. degree from the Computer Science and Engineering Department, University of California, San Diego, CA, USA, in 2002.

In 2002, she joined the Electrical and Computer Engineering Department, Duke University, Durham, NC, USA, as an Assistant Professor. She worked on testing mixed-signal and radio frequency circuits, built-in-self test techniques, analysis and mitigation of process variations, defect-tolerant microprocessor systems, and online, and offline testing of microfluidic devices. In August 2008, she joined the Electrical Engineering Department, Arizona State University, Tempe, AZ, USA, as an Associate Professor, continuing on the same line of research. She has published over 70 conference and journal papers and holds one U.S. patent.

Dr. Ozev was a recipient of an NSF CAREER Award in 2006, and various other awards from NSF, SRC, NASA, and IBM. She also received the Best Dissertation Award from UCSD in 2002, the Best Paper Award from IEEE International Conference on Computer Design in 2005, the TTTC Naveena Nagi Award at VTS in 2002, and the Best Session Award at VTS in 2006.



David Z. Pan (S'97–M'00–SM'06) received the B.S. degree from Peking University, Peking, China, and the M.S. and Ph.D. degrees from University of California, Los Angeles (UCLA), CA, USA.

From 2000 to 2003, he was a Research Staff Member with IBM T. J. Watson Research Center. He is currently an Associate Professor with the Department of Electrical and Computer Engineering, the University of Texas at Austin, Austin, TX, USA. He has published over 140 papers in international conferences and journals, and holds 8 U.S. patents. His research interests include nanometer physical design, design for manufacturability and reliability, vertical integration design and technology, and design/CAD for emerging technologies.

Dr. Pan has served as an Associate Editor for the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS, the *Journal of Computer Science and Technology*, and the *IEEE CAS Society Newsletter*. He has served as the Chair of the IEEE CANDE Committee and the ACM/SIGDA Physical Design Technical Committee (PDTC). He is in the Design Technology Working Group of International Technology Roadmap for Semiconductor. He has served in the Technical Program Committees of major VLSI/CAD conferences, including ASPDAC (Track Chair), DAC (Track Chair), DATE, ICCAD, ISPD (Program Chair), ISQED (Topic Chair), ISCAS (CAD Track Chair), SLIP (Publication Chair), GLSVLSI, ACISC (Program Co-chair), ICICDT (Award Chair), and VLSI-DAT (EDA Track Chair). He is the General Chair of ISPD 2008, General Chair of ACISC 2009, and Steering Committee Chair of ISPD 2009. He was a recipient of a number of awards for his research contributions and professional services, including ACM/SIGDA Outstanding New Faculty Award (2005), NSF CAREER Award (2007), SRC Inventor Recognition Award three times (2000 and 2008), IBM Faculty Award four times (2004–2006, 2010), UCLA Engineering Distinguished Young Alumnus Award (2009), Best Paper Award at ASPDAC 2010, Best IP Award at DATE 2010, SRC Techcon Best Paper in Session Award (1998 and 2007), Best Student Paper Award at ICICDT 2009, IBM Research Bravo Award (2003), Dimitris Chorafas Foundation Research Award (2000), ISPD Routing Contest Awards (2007), eASIC Placement Contest Grand Prize (2009), a number of Best Paper Award Nominations at DAC/ICCAD/ASPAC/ISPD, and ACM Recognition of Service Award (2007 and 2008). He is a Cadence Distinguished Speaker in 2007 and IEEE CAS Society Distinguished Lecturer for 2008–2009.



Zebo Peng (M'91–SM'02) received the B.Sc. degree in computer engineering from the South China Institute of Technology, China, in 1982, and the Licentiate of Engineering and Ph.D. degrees in computer science from Linköping University, Linköping, Sweden, in 1985 and 1987, respectively.

He is currently a Full Professor of Computer Systems, Director of the Embedded Systems Laboratory, and Chairman of the Division for Software and Systems in the Department of Computer Science, Linköping University. He served as the Director of the National Graduate School of Computer Science, Sweden, from 2006 to 2008. His current research interests include design and test of embedded systems, electronic design automation, SoC testing, fault tolerant design, hardware/software codesign, and real-time systems. He has published more than 250 technical papers, and coauthored 4 books: *System Synthesis with VHDL* (Kluwer, 1997), *Analysis and Synthesis of Distributed Real-Time Embedded Systems* (Kluwer, 2004), *System-Level Test and Validation of Hardware/Software Systems* (Springer, 2005), and *Real-Time Applications with Stochastic Task Execution Times*

(Springer, 2007).

Prof. Peng was a recipient of two Best Paper Awards at the European Design Automation Conferences (1992 and 1994), a Best Paper Award at the IEEE Asian Test Symposium (2002), a Best Paper Award at the Design Automation and Test in Europe Conference (2005), and a Best Presentation Award at the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (2003). He serves currently as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, the *VLSI Design Journal*, and the *EURASIP Journal on Embedded Systems*. He served as the Guest Editor for the Special Issue on “Emerging Strategies for Resource-Constrained Testing of System Chips” in the *IEEE Proceedings for Computer and Digital Techniques* and the special issue on “Design Methodologies and Tools for Real-Time Embedded Systems” in the *Journal on Design Automation for Embedded Systems*. He has served on the program committee of a dozen international conferences and workshops, including ATS, DATE, DDECS, DFT, ETS, IOLTS, MEMOCDE, RTCSA, and VLSI-SOC. He was the Program Chair of the 7th IEEE Design and Diagnostics of Electronic Circuits and Systems Workshop (DDECS 04), the 12th IEEE European Test Symposium (ETS 07), and the 11th Design Automation and Test in Europe Conference (DATE 08). He served as the Chair of the IEEE European Test Technology Technical Council (ETTTC) in 2006–2009, and has been a Golden Core Member of the IEEE Computer Society since 2005.

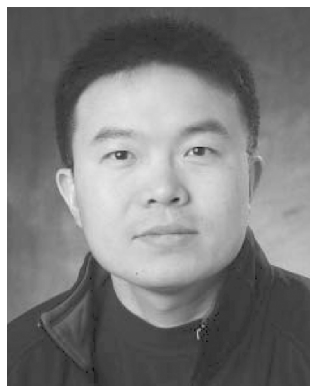


Emre Salman received the B.S. degree in microelectronics engineering from Sabanc University, Istanbul, Turkey, in 2004, and the M.S. and Ph.D. degrees in electrical engineering from the University of Rochester, Rochester, NY, USA, in 2006 and 2009, respectively.

He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Stony Brook University, Stony Brook, NY, USA. Between October 2003 and May 2004, he was with STMicroelectronics, Istanbul, Turkey, where he contributed to the design and verification of an ultra low power clock and data recovery circuit for a multichannel fiber-optic transceiver. In the Summer of 2005, he was with Synopsys Inc., Mountain View, CA, USA, where he worked on pessimism reduction in static timing analysis (STA) and cell library characterization. During the Summers of 2006 and 2007, he was with Freescale Semiconductor, Tempe, AZ, USA, developing circuit- and physical-level signal isolation methodologies with application to monolithic transceivers in CMOS and BiCMOS technologies. He also worked as a post doctoral research associate with the University of Rochester, between May 2009 and August 2010. His research interests

include analysis, modeling, and design methodologies for high-performance digital and mixed-signal heterogeneous integrated circuits; physical design techniques to enhance signal/power integrity, robustness, and reliability; and emerging integrated circuit technologies. He has published over 20 publications in peer reviewed journals and conferences and holds two issued U.S. patents.

Dr. Salman is currently an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, *Journal of Circuits, Systems, and, Computers* (JCSC), and the *Journal of Low Power Electronics and Applications* (JLPEA). He also serves on the technical program committee of the ACM/SIGDA Great Lakes Symposium on VLSI (GLSVLSI) and Asia Symposium on Quality Electronic Design (ASQED).



Li Shang received the Ph.D. degree from Princeton University, Princeton, NJ, USA, and the B.E. degree with honors from Tsinghua University, Beijing, China.

He is currently the Chief Architect of Intel Labs, China. He has been an Assistant Professor with the Department of Electrical, Computer, and Energy Engineering, University of Colorado, Boulder, CO, USA. He has published in the areas of embedded systems, design automation, design for nanotechnologies, distributed computing, and computer architecture.

Dr. Shang was a recipient of the Provost's Faculty Achievement Award, University of Colorado 2010, NSF CAREER Award 2010, the Best Paper Award at DATE 2010, and the Best Paper Award at PDCS 2002. He was also a recipient of his department's Teaching Award in 2006. His work on temperature-aware on-chip network has been selected for publication in MICRO Top Picks 2006. His recent work has also been nominated for the Best Paper Award at ISLPED 2010, ICCAD 2008, DAC 2007, and ASP-DAC 2006. He is currently serving as an Associate Editor of *ACM Journal on Emerging Technologies in Computer Systems*, and serves on the technical program committees

of several embedded systems, design automation, VLSI, and computer architecture conferences.



Ankur Srivastava received the Bachelor's in Technology degree in electrical engineering from the Indian Institute of Technology, Delhi, in 1998, the Master's degree in computer engineering from the Department of Electrical and Computer Engineering, Northwestern University, Evanston, IL, USA, in June 2000, and the Ph.D. degree from the Computer Science Department, University of California, Los Angeles, CA, USA, in 2002.

He is an Associate Professor with the Electrical and Computer Engineering Department, University of Maryland, College Park, MD, USA, with a joint appointment with the Institute for Systems Research. He has been working at the University of Maryland since October 2002. His main area of interest is VLSI CAD for high performance and low power VLSI circuits.

Dr. Srivastava was a recipient of the "Outstanding Ph.D. Award" from the Computer Science Department of UCLA and the George Corcoran Memorial Outstanding Teaching Award by the ECE Department of University of Maryland.



Syng-Jyan Wang (S'90–M'92) received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1984, and the Ph.D. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 1992.

From 1984 to 1986, he was a Reserve Officers' Training Corps Officer with the Air Force, Taiwan. From 1986 to 1987, he was a Teaching Assistant with the Department of Electrical Engineering, National Taiwan University. He was a Consultant with AT&T Bell Laboratories, Holmdel, NJ, USA, from 1989 to 1990. Since 1992, he has been with the Department of Computer Science and Engineering, National Chung Hsing University (NCHU), Taichung, Taiwan, where he was the Chair from 1999 to 2005 and where he is currently a Professor. His research interests include digital testing, low-power design, and computer-aided design of VLSI systems.

Dr. Wang has been serving on the technical program committees of IEEE Asian Test Symposium (ATS) and IEEE International Symposium on VLSI Design, Automation, and Test (VLSI-DAT). He has also served as Program Chair for ATS 2009.



Zhongfeng Wang received the B.E. and M.S. degrees from the Department of Automation, Tsinghua University, Beijing, China, and the Ph.D. degree from the Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN, USA, in 2000.

In the past, he has worked for Beijing Hua-hai New Technology Development Co., Beijing, China, Morphics Technology Inc. (now a part of Infineon Technology), Campbell, CA, National Semiconductor Co., Longmont, CO, USA. From 2003 to 2007, he worked as an Assistant Professor with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR, USA. Since 2007, he has been working for Broadcom Corporation, Irvine, CA, USA, as a Senior Principle Scientist. He has edited one book "VLSI" (InTech), authored/coauthored over 100 international journal and conference papers, and filed numerous patent applications and disclosures. His research interests include the areas of digital signal processing, digital communications and networking, and low power/high speed VLSI implementation.

Dr. Wang was the recipient of the IEEE Circuits and Systems (CAS) Society VLSI Transactions Best Paper Award in 2007 and the Best Student Paper Award at the 1999 IEEE Workshop on Signal Processing Systems (SiPS'99). He has coauthored three papers ranking among top 10 most downloaded manuscripts in IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS from 2007 to 2009. He has served as Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS (2004–2005), the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS (2008–2011), and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (2009–2012). He has also served in many technical program committees and technical committees in the IEEE CAS Society and IEEE Signal Processing Society.



Yuan Xie received the B.S. degree in electronic engineering from Tsinghua University, Beijing, China, and the M.S. and Ph.D. degrees in electrical engineering from Princeton University, Princeton, NJ, USA.

He is an Associate Professor with the Computer Science and Engineering Department, Pennsylvania State University (Penn State), University Park. Before joining Penn State in Fall 2003, he was with IBM Microelectronic Division's Worldwide Design Center, Essex Junction, VT, USA. He has published over 130 conference and journal papers, on topics including VLSI design, computer architecture, design automation, and embedded system designs.

Dr. Xie was a recipient of the SRC Inventor Recognition Award, the National Science Foundation Early Faculty (CAREER) Award, IBM Faculty Award, NSFC Overseas, and Hong Kong Macau Young Scholars Collaborative Research Award, and several Best Paper Award and Best Paper Award Nominations at IEEE/ACM conferences. He is an ACM Distinguished Speaker and IEEE Computer Society Distinguished Visitor. He served as an Associate Editor for the IEEE

TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS, the *IEEE Design and Test of Computers*, the *ACM Journal of Emerging Technologies in Computing Systems*, and the *IET Computers and Digital Techniques*.



Jiang Xu (S'02–M'07) received the B.S. and M.S. degrees in electrical engineering from Harbin Institute of Technology, Harbin, China, in 1998 and 2000, and the M.A. and Ph.D. degrees in electrical engineering from Princeton University, Princeton, NJ, USA, in 2002 and 2007, respectively.

From 2001 to 2002, he worked with Bell Labs, Holmdel, NJ, USA, as a Research Associate and discovered the First Generation Dilemma in platform-based SoC design methodologies. He was a Research Associate with NEC Laboratories America, from 2003 to 2005 and working on network-on-chip designs and implementations. He joined a startup company, Sandbridge Technologies, from 2005 to 2007 and worked on the development and implementation of two generations of ultra-low power multiprocessor systems-on-chip for mobile platforms. In 2007, he joined the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong, as an Assistant Professor, where he established the Mobile Computing System Lab. He authored or coauthored more than 40 book chapters and papers in peer-reviewed journals and international conferences. He coauthored a book titled *Algorithms, Architecture and*

System-on-Chip Design for Wireless Applications (to be published by Cambridge Univ. Press). His research areas include network-on-chip, multiprocessor system-on-chip, embedded system, computer architecture, low-power VLSI design, and HW/SW codesign.

Dr. Xu is currently serving as an Associate Editor of the *ACM Transactions on Embedded Computing Systems* and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He is an ACM Distinguished Speaker since 2010 and a Distinguished Visitor of IEEE Computer Society from 2011 to 2013. He served on the organizing and technical committees in many international conferences, including ICCD, CASES, ISVLSI, VLSI, EMSOFT, VLSI-SoC, ICSS, RTCSA, NOCS, ASP-DAC, etc. He was a recipient of a Best Paper Award and a Best Poster Award.



Hai Zhou received the B.S. and M.S. degrees in computer science and technology from Tsinghua University, Beijing, China, in 1992 and 1994, respectively, and the Ph.D. degree in computer sciences from the University of Texas at Austin, Austin, TX, USA, in 1999.

He is an Associate Professor with the Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, IL, USA. His research interests include VLSI computer-aided design, algorithm design, and formal methods.

Dr. Zhou was a recipient of a CAREER Award from the National Science Foundation in 2003.



Stacey Weber Jackson received the B.A. degree in sociology and the M.S.W. degree in social work from Rutgers University, New Brunswick, NJ, USA, in 1998 and 2002, respectively.

She is a New Jersey State Certified Social Worker. She is currently serving as the Editorial Assistant for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.