Editorial
Appointments for 2005–2006 Term

I AM extremely pleased to announce the editorial board appointments for the term 2005–2006 with the inclusion of new members. The appointment of new members adds to the breadth and diversity of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and we are quite proud of the energy and the enthusiasm radiated by the new members who have been serving on the board already for sometime this year. It can be noticed that some of the associate editors will be completing their terms and so not included here. However, they will continue to serve as Associate Editors until they complete the processing of the manuscripts they are already handling. We are extremely grateful to all of the Associate Editors for their outstanding work during the past two and half years. The quality of the editorial process largely depends on the Associate Editors and we have been very fortunate.

I am happy to note that Dr. Srimat Chakradhar has kindly agreed to continue as the Associate Editor-In-Chief and his knowledge of the field as well as his vast experience in terms of the review process having served numerous times as program chair and on program committees has been a great source to look for help and advice whenever I have needed. Further, Michael Pham has agreed to continue to serve as the Editorial Assistant for the new term and it is needless to say that he has been a great asset to me and TVLSI in keeping things flowing smooth from an organizational perspective. Two other persons that come to my mind who have always been providing tremendous service to TVLSI are Mona Mittra at the publications office and Denise Hurley at IEEE. The announcement of the new editorial board has been overdue for sometime and I apologize for the delay in getting all the formalities completed. A few suggestions have been made by some of the editors and authors and we are about to begin a discussion among the editors and the steering committee members on how to improve the process overall so we can better serve the VLSI community. Please feel free to send a note to me or Dr. Chakradhar anytime.

The biographies and photographs of the members of the Editorial Board for 2005–2006 term are listed in the following pages.

NAGARAJAN RANGANATHAN, *Editor-in-Chief*
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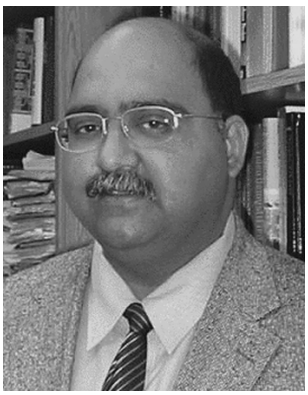


Nagarajan Ranganathan (S'81–M'88–SM'92–F'02) received the B.E. (hons.) degree in electrical and electronics engineering from Regional Engineering College, Tiruchirapalli, University of Madras, India, and the Ph.D. degree in computer science from the University of Central Florida, Orlando, in 1983 and 1988, respectivley.

He is currently a Professor in the Department of Computer Science and Engineering and the Nanomaterials and Nanomanufacturing Research Center at the University of South Florida, Tampa. His research interests include very large scale integration (VLSI) system design, design automation, power estimation and optimization, high level synthesis, embedded systems, and computer architecture. He has developed many special purpose VLSI chips for computer vision, image processing, pattern recognition, data compression, and signal processing applications. He has published over 190 papers in reputed journals and conferences and is a co-owner of five U.S. patents related to application specific integrated circuits and has recently filed for two patents, one on a new technique for leakage reduction in CMOS circuits and other for a virtual reality navigation system for learning human anatomy.

Dr. Ranganathan was elected as Fellow of IEEE in 2002 for his contributions to "algorithms and architectures for VLSI systems." He received the Theodore–Venette Askounes Ashford Distinguished Scholar Award at the University of South Florida in 2003. He served as the Chair of the IEEE Computer Science Technical Committee on VLSI during 1997–2000. He has served on the Program Committees of international conferences such as ICCD, ISLPED, CAMP, ICPP, IPPS, SPDP, VLSI Design, and ICHPC. He has served on the editorial boards of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING, and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY. He has served on the editorial boards of *Pattern Recognition* and the *International Journal of VLSI Design*. He served as the Steering Committee Chair for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, during 2000–2002. He is currently serving as the Editor-in-Chief of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS for two consecutive terms 2003–2006.

Vishwani D. Agrawal (M'70–SM'80–F'86) received the B.E. degree from the University of Roorkee, Roorkee, India, in 1964, the M.E. degree from the Indian Institute of Science, Bangalore, India, in 1966, and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign, in 1971.

He has over 30 years of industry and university experience, working at Bell Labs, Murray Hill, NJ; Rutgers University, New Brunswick, NJ; TRW, Redondo Beach, CA; IIT, Delhi, India; EG&G, Albuquerque, NM; and ATI, Champaign, IL. His areas of expertise include VLSI testing, low-power design, and microwave antennas. He recently retired from Agere Systems to pursue a full-time academic and consulting career. Currently, he is an adjunct Visiting Professor of Electrical and Computer Engineering at Rutgers University, New Brunswick, NJ, a position he has held since 1990. Intensely interested in education and research, he serves on the Advisory Boards of the Electrial and Computer Engineering Departments of the University of Illinois and the New Jersey Institute of Technology, teaches at Rutgers University, and has directed the Ph.D. dissertation research of students at various universities including Berkeley, Carnegie Mellon University (CMU), Illinois, Nebraska, Rutgers, and Wisconsin. He is a Co-Principal Investigator for two NSF grants to the Electrial and Computer Engineering Department at Rutgers University. He has published over 250 papers, has coauthored five books, and holds 13 U.S. patents. His text book, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits* (Norwell, MA: Kluwer, 2000), co-authored with M. L. Bushnell, was recently published. He is the founder and Consulting Editor of the Frontiers in Electronic Testing book series of Kluwer Academic Publishers, Boston. He is a co-founder of the International Conference on VLSI Design, and the International Workshops on VLSI Design and Test, held annually in India. He has served on numerous conference committees and is a frequently invited speaker. He was the invited Plenary Speaker at the 1998 International Test Conference, Washington, DC, and the Keynote Speaker at the 9th Asian Test Symposium, held in Taiwan, R.O.C., in 2000.

Dr. Agrawal is the founder and Editor-in-Chief (since 1990) of the *Journal of Electronic Testing: Theory and Applications*, and a past Editor-in-Chief (1985–1987) of the *IEEE Design and Test of Computers* magazine. During 1989 and 1990, he served on the Board of Governors of the IEEE Computer Society. He has received seven Best Paper Awards and one Honorable Mention Paper Award. In 1998, he received the Harry H. Goode Memorial Award of the IEEE Computer Society for "innovative contributions to the field of electronic testing," and in 1993, received the Distinguished Alumnus Award of the University of Illinois at Urbana-Champaign, "in recognition of his outstanding contributions in design and test of VLSI systems." He is a Fellow of IETE-India (elected in 1983) and a Fellow of the ACM (elected in 2003).

Srimat T. Chakradhar received the Ph.D. degree in computer science from Rutgers University, New Brunswick, NJ, in 1990.

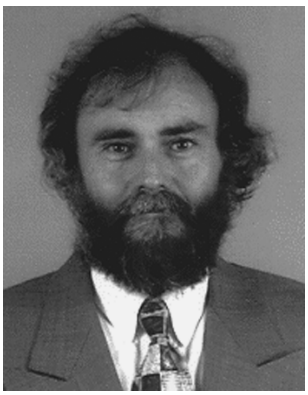
He is currently a Department Head at NEC Laboratories America, Inc., Princeton, NJ. During 1989, he also worked at the AT&T Bell Laboratories, Murray Hill, NJ. His current research interests include design and test of hardware and software for networked computing systems, electronic design automation, wireless and embedded systems, and system-on-a-chip designs. He has been awarded more than 50 U.S. and international patents (Japan and Europe) in computing systems software and hardware. He has published one book and over 100 technical papers in refereed journals and conference proceedings. He has also served as a thesis advisor for four Ph.D. dissertations from reputed U.S. universities.

Dr. Chakradhar has received five Best Paper Awards and four award nominations at premier international conferences of the ACM and IEEE (including the Design Automation Conference) for his work on design and test of computing systems. He has successfully organized and served on the board of several international conferences organized by the ACM or IEEE, in various capacities including General Chair and Technical Program Chair. He has served as guest editor for numerous IEEE publications and he is presently the Associate Editor for *Journal on Electronic Testing*.

Krishnendu Chakrabarty (S'92–M'96–SM'00) received the B.Tech. degree in computer science and engineering from the Indian Institute of Technology, Kharagpur, in 1990, and the M.S.E. and Ph.D. degrees in computer science and engineering from the University of Michigan, Ann Arbor, in 1992 and 1995, respectively, all in computer science and engineering.

He is currently Associate Professor of electrical and computer engineering at Duke University, Durham, NC. He is a coauthor of two books: *Microelectrofluidic Systems: Modeling and Simulation* (Boca Raton, FL: CRC, 2002) and *Test Resource Partitioning for System-on-a-Chip* (Norwell, MA: Kluwer, 2002), and the Editor of *SOC (System-on-a-Chip) Testing for Plug and Play Test Automation* (Norwell, MA: Kluwer, 2002). He is also a coauthor of the forthcoming book *Scalable Infrastructure for Distributed Sensor Networks* (London, U.K.: Springer). He has published over 190 papers in journals and refereed conference proceedings, and he holds a U.S. patent in built-in self-test. His current research projects include the design and testing of system-on-chip integrated circuits; embedded real-time systems; distributed sensor networks; design automation of microfluidics-based biochips; and microfluidics-based chip cooling.

Dr. Chakrabarty is a member of ACM and ACM SIGDA, and a member of Sigma Xi. He is an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and he served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING. He is an Associate Editor of *ACM Journal on Emerging Technologies in Computing Systems* and Editor of the *Journal of Electronic Testing: Theory and Applications* (*JETTA*). He serves as a subject area editor for the *International Journal of Distributed Sensor Networks*. He is a Distinguished Visitor of the IEEE Computer Society for 2005–2007. He serves as Vice Chair of Technical Activities in IEEE's Test Technology Technical Council, and is a member of the program committees of several IEEE/ACM conferences and workshops. He served as the Tutorial Co-Chair for the 2005 IEEE International Conference on VLSI Design and is the designated Program Co-Chair for the 2005 IEEE Asian Test Symposium. He is a recipient of the National Science Foundation Early Faculty (CAREER) award and the Office of Naval Research Young Investigator award. He is a recipient of a best paper award at the 2001 Design, Automation and Test in Europe (DATE) Conference. He is also a recipient of the Humboldt Research Fellowship from the Alexander von Humboldt Foundation, Germany.



Bernard Courtois (M'92) received the Engineer degree in 1973 from the Ecole Nationale Supérieure d'Informatique et Mathématiques Appliquées de Grenoble, Grenoble, France, and the "Docteur-Ingénieur" and "Docteur-ès-Sciences" degrees from the Institut National Polytechnique de Grenoble, Grenoble, France.

He is currently the Director of the Laboratory of Techniques of Informatics and Microelectronics for Computer Architecture (TIMA) where researches include CAD, and architecture and testing of integrated circuits and systems. He is also the Director of CMP Service for Universities and Companies from about 60 countries for ICs, MCMs, and MEMS prototyping and small volume production. He has been General Chair or Program Chair of various international conferences and workshops, including EDAC-ETC-EUROASIC, Electron and Optical Beam Testing, EUROCHIP, Mixed-Signal Testing, Rapid System Prototyping, THERMINIC, Design, Test and Microfabrication of MEMS/MOEMS and POLYTRONIC. He is Doctor Honoris Causa of the Technical University of Budapest.

Dr. Courtois is a member of ACM, ASME, and IMAPS. He is a IEEE Computer Society's Golden Core Member.

Ronald DeMara (M'95) received the B.S. degree (hons.) in electrical engineering from Lehigh University, Bethlehem, PA, in 1987, the M.S. degree in electrical engineering from the University of Maryland, College Park, in 1989, and the Ph.D. degree in computer engineering from the University of Southern California, Los Angeles, in 1992.

After serving as an Associate Engineer at IBM for a few years he joined the University of Central Florida, Orlando, in 1993, where he is presently an Associate Professor in the Computer Engineering Program of SEECS. He has served as the Program Coordinator for the Computer Engineering Program and has developed three different courses during his teaching career. He has over 43 publications in conference proceedings, journals, and book chapters and has been the principal investigator and co-principal investigator in more than 14 research projects so far.

Dr. DeMara is a reviewer for National Science Foundation, *Journal of Parallel and Distributed Computing,* IEEE TRANSACTIONS ON PARALLEL AND DISTRIBUTED COMPUTING, ICPP, ISCA, IPPS, and AAAI.

Xiaobo Sharon Hu (S'85–M'89–SM'02) received the B.S. degree from Tianjin University, China, the M.S. degree from the Polytechnic Institute of New York, Brooklyn, and the Ph.D. degree from Purdue University, West Lafayette, IN.

She is an Associate Professor in the Department of Computer Science and Engineering, University of Notre Dame, Notre Dame, IN. She was with General Motors Research Laboratories, Warren, MI, as Senior Research Engineer, and at Western Michigan University, Kalamazoo, as Assistant Professor. Her research interests include hardware–software codesign, real-time embedded systems, low-power system design, and design automation algorithms. She has published more than 70 papers in the related areas.

Dr. Hu has served on the Program Committee of a number of Conferencea such as DAC, ICCAD, DATE, CODES, ICCD, and GVLSI. She was the Program Co-Chair of CODES in 2001, and the General Co-Chair of the same conference in 2002. She received the NSF CAREER Award in 1997 and the Best Paper Award at the 38th Design Automation Conference in 2001.

Yehea I. Ismail (M'00) was born in Giza, Egypt, on November 11, 1971. He received the B.Sc. and M.S. degree in electronics and communications engineering with distinction and honors from Cairo University, Cairo, Egypt. in 1993 and 1996, respectively, the M.S. and Ph.D. degrees from the University of Rochester, Rochester, NY, in 1998 and 2000, repectively.

In August 1993, as one of the top of his class, he was appointed as a Teacher Assistant, in the Department of Electrical and Computer Engineering, Cairo University. He is currently an Assistant Professor with Northwestern University, Evanston, IL. He was with IBM Cairo Scientific Center (CSC), from 1993 to 1996, and with IBM Microelectronics, Fishkill, NY, from 1997 to 1999. He has authored more than 50 technical papers and a book. His primary research interests include interconnect, noise, innovative circuit simulation, and related circuit level issues in high-performance VLSI circuits.

Prof. Ismail is on the Editorial Board of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, on the Editorial Board of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: FUNDAMENTAL THEORY AND APPLICATIONS, and a Guest Editor for a special issue of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS on "On-Chip Inductance in High Speed Integrated Circuits." He was selected as the 2002 IEEE Circuits and Systems Society Outstanding Young Author Award Winner. He also won the National Science Foundation Career Award in 2002. He was given the Best Teacher Award from the Electrical and Computer Engineering Department, Northwestern University, Evanston, IL, in 2003.

Niraj K. Jha (S'85–M'85–SM'93–F'98) received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, in 1981, the M.S. degree in electrical engineering from the State University of New York, Stony Brook, in 1982, and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign, in 1985.

He is currently a Professor of electrical engineering with Princeton University, Princeton, NJ. His research interests include low-power hardware and software design, computer-aided design of integrated circuits and systems, digital system testing, and distributed computing. He is the Director of the Center for Embedded System-on-a-Chip Design, which is funded by New Jersey Commission on Science and Technology. He has coauthored *Testing and Reliable Design of CMOS Circuits* (Norwell, MA: Kluwer, 1990), *High-Level Power Analysis and Optimization* (Norwell, MA: Kluwer, 1998), and *Testing of Digital Systems* (Cambridge, U.K.: Cambridge Univ. Press, 2003). He has also authored three book chapters and authored or coauthored over 250 technical papers. He holds 11 U.S. patents. He is currently the Editor of the *Journal of Electronic Testing: Theory and Applications* (*JETTA*), and the *Journal of Embedded Computing* and has served as a Guest Editor for the *JETTA* "Special Issue on High-Level Test Synthesis."

Prof. Jha is a Fellow of the Association for Computing Machinery. He has served as an associate editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS —II: ANALOG AND DIGITAL SIGNAL PROCESSING. He is currently editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He has also served as the program chairman of the 1992 Workshop on Fault-Tolerant Parallel and Distributed Systems and the 2004 International Conference on Embedded and Ubiquitous Computing. He was the recipient of the AT&T Foundation Award and NEC Preceptorship Award for research excellence, the NCR Award for teaching excellence, and the Princeton University Graduate Mentoring Award. He has coauthored six papers, which have earned the Best Paper Award at ICCD'93, FTCS'97, ICVLSID'98, DAC'99, PDCS'02, and ICVLSID'03. Another paper of his was selected for "The Best of ICCAD: A collection of the best IEEE International Conference on Computer-Aided Design papers of the past 20 years."

Lizy Kurian John (M'00) received the B.S. degree in electronics and telecommunication from University of Kerala, India, and the M.S. degree in computer engineering from University of Texas, El Paso, and the Ph.D. degree in computer engineering from The Pennsylvania State University, State College, in 1993.

She is currently an Associate Professor in the Electrical and Computer Engineering Department at Univerity of Texas (UT), Austin, and is a UT Austin Engineering Foundation Centennial Teaching Fellow. Prior to joining UT Austin in 1996, she was on the faculty at University of South Florida, Tampa. Her research interests include high performance processor and memory architectures, low power design, reconfigurable architectures, rapid prototyping, field programmable gate arrays, and workload characterization. She has published papers in the IEEE TRANSACTIONS ON COMPUTERS, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, ACM/IEEE International Symposium on Computer Architecture (ISCA), IEEE Micro Symposium (MICRO), IEEE High Performance Computer Architecture Symposium (HPCA), ACM International Symposium on Low Power Electronics and Design (ISLPED), and has a patent for a field programmable memory cell array chip. Her research has been supported by the National Science Foundation, the State of Texas Advanced Technology program, DARPA, IBM, Intel, Motorola, DELL, AMD and Microsoft Corporations.

Dr. John has received the NSF CAREER award, Junior Faculty Enhancement Award from Oak Ridge Associated Universities, IBM Austin Center for Advanced Studies (CAS) Fellowship, UT Austin Engineering Foundation Faculty Award (2001), Halliburton, Brown and Root Engineering Foundation Young Faculty Award (1999), etc. She is a Member of the IEEE Computer Society and ACM and ACM SIGARCH. She is also a Member of Eta Kappa Nu, Tau Beta Pi, and Phi Kappa Phi.

Ming-Dou Ker (S'92–M'94–SM'97) received the B.S. degree in electronics engineering and the M.S. and Ph.D. degrees from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1986, 1988, and 1993, respectively.

In 1994, he joined the Very Large Scale Integration (VLSI) Design Department, Computer and Communication Research Laboratories (CCL), Industrial Technology Research Institute (ITRI), Taiwan, R.O.C., as a Circuit Design Engineer. In 1998, he became a Department Manager with the VLSI Design Division, CCL/ITRI. In 2000, he became an Associate Professor with the Department of Electronics Engineering, National Chiao-Tung University. He has been invited to teach or help ESD protection design and latchup prevention by hundreds of design houses and semiconductor companies in Hsinchu, Taiwan, R.O.C., and in Silicon Valley, San Jose, CA. His research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed or mixed-voltage I/O interface circuits, especial sensor circuits, and semiconductors. In the field of reliability and quality design for CMOS ICs, he has authored or coauthored over 200 technical papers in international journals and conferences. He holds over 180 patents on reliability and quality design for ICs, which including 81 U.S. patents. His inventions on ESD protection design and latchup prevention method have been widely used in modern IC products.

Dr. Ker has served as member of the Technical Program Committee and Session Chair of numerous international conferences (including IEEE ISCAS, IEEE AP-ASIC, IEEE SOC, IEEE IRPS, IEEE ISQED, IPFA, EOS/ESD Symposium, VLSI-TSA, IECMAC,). He has served as the Chair ofRF ESD committee of 2004 International EOS/ESD Symposium, and the Vice-Chair of Latchup committee for 2005 IEEE International Reliability and Physics Symposium (IRPS). He also served as the Technical Program Committee Chair of 2002 Taiwan ESD Conference, the General Chair of 2003 Taiwan ESD Conference, the Publication Chair of 2004 IPFA, Steering Committee of 2004 IPFA, and the ESD Program Chair of 2004 International Conference on Electromagnetic Applications and Compatibility. He was the Organizer of the Special Session on ESD Protection Design for Nanoelectronics and Gigascale Systems in ISCAS 2005. Recently, he was invited as the supervisor to the Standard I/O Committee in the Fabless Semiconductor Association (FSA). He also served as active reviewers for many IEEE Transactions and Journals (ED, EDL, DMR, CPT, JSSC, CAS, VLSI). In 2001, he set up the Taiwan ESD Association. He was elected as the first President of Taiwan ESD Association in 2001. Dr. Ker has received many research awards from ITRI, National Science Council, National Chiao-Tung University, and the Dragon Thesis Award from Acer Foundation. In 2003, he was selected as one of the Ten Outstanding Young Persons in Taiwan by Junior Chamber International (JCI).

Israel Koren (M'75–SM'87–F'91) received the B.Sc., M.Sc., and D.Sc. degrees from the Technion—Israel Institute of Technology, Haifa, Israel, in 1967, 1970, and 1975, respectively, all in electrical engineering.

He is currently a Professor of Electrical and Computer Engineering at the University of Massachusetts, Amherst. Previously he held positions with the Technion—Israel Institute of Technology, Haifa, the University of California at Berkeley, the University of Southern California, Los Angeles, and the University of California, Santa Barbara. He has been a consultant to several companies including Analog Devices, AMD, Digital Equipment Corporation, IBM, Intel, National Semiconductor, and Tolerant Systems. His current research interests are models for yield of VLSI circuits, techniques for yield and reliability enhancement, fault-tolerant architectures, real-time systems and computer arithmetic. He has edited and co-authored the book, *Defect and Fault-Tolerance in VLSI Systems* (New York: Plenum, 1989). He is the author of the textbook *Computer Arithmetic Algorithms* (Natick, MA: A. K. Peters, 2002, 2nd ed.). He has published extensively in the IEEE Transactions.

Dr. Koren has been a Co-Guest Editor for the IEEE TRANSACTIONS ON COMPUTERS, the Special Issue on Computer Arithmetic, July 2000, and the Special Issue on High Yield VLSI Systems, April 1989. He has served on the Editorial Board during 1992–1997. He also served as General Chair, Program Chair, and Program Committee Member for numerous conferences.

Bin-Da Liu (S'79–M'82–SM'95) received the B. S., M. S., and Ph.D. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan, R.O.C., in 1973, 1975, and 1983, respectively.

From 1975 to 1977, he served as an Electrical Officer in the Combined Service Forces. Since 1977, he has been on the faculty of the National Cheng Kung University, where he is currently a Professor in the Department of Electrical Engineering. From 1983 to 1984, he was a Visiting Assistant Professor in the Department of Computer Science, University of Illinois at Urbana-Champaign. From 1988 to 1992, he was the Director of Electrical Laboratories, National Cheng Kung University. He was the Associate Chairman of the Electrical Engineering Department from 1996 to 1999 and the Chairman from 1999 to 2002. From 1990 to 1993, he was a member of the Evaluation Committee for the Junior Engineering College, Ministry of Education. Since 1995, he has been a Consultant with the Chip Implementation Center, National Science Council. Since 2002, he has been the Coordinator of the Digital IP Consortium, VLSI Educational Program of Ministry of Education and the Coordinator of the SoC Design Promotion Program of National Science Council. He organized the Taiwan Student VLSI Design Contest in 1998, 1999, and 2000. He has published more than 170 technical papers and has contributed chapters in the book *Neural Networks and Systolic Array Design* (Singapore: World Scientific, 2002) and the book *Trade-Off Between Accuracy and Interpretability in Fuzzy Rule-Based Modeling* (Heidelberg, Germany: Springer-Verlag, 2002). His current research interests include physical design and testing for VLSI circuits, system-on-chip (SoC) system integration and verification, and VLSI implementation for fuzzy-neural networks and video signal processors.

Dr. Liu is a member on the Board of Governors of Taiwan IC Design Society and a member of Phi Tau Phi, Taiwan SOC Consortium, International Union of Radio Science, Chinese Fuzzy Systems Association, and Chinese Institute of Electrical Engineering (CIEE). He was the Chair of IEEE Circuits and Systems Society—Taipei Chapter during 2003–2004. He received Dragon Distinguished Paper Award from the Acer Foundation in 1991, 1997, and 2004, the Best Paper Award from the CIEE in 1995 and 2002, the Golden Silicon Award from the Macronix Foundation in 2001, 2002, and 2003, the MPC Chip Design Award from the National Chip Implementation Center in 2002, 2003, and 2004, the Low Power Design Contest Award form the ACM/IEEE in 2003, the Shen Wen-Zen Memorial Paper Award from the Taiwan IC Design Society in 2004, the Outstanding Electrical Engineering Professor Award from the CIEE in 2004, the Lam Research Thesis Award from Lam Research Corporation, and the Research Award from the National Science Council annually since 1988. He organized the Taiwan Student VLSI Design Contest in 1998, 1999, and 2000. Since 1992, he has served as a Member of the Steering Committee of VLSI Design/CAD Symposium and served as the General Chair in 1994. He served as a member of the Technical Program Committee of the 1998 and the 1999 IEEE Workshop on VLSI Signal Processing Systems, the 1998 and the 2000 IEEE Asia Pacific Conference on Circuits and Systems, the First, the Second, and the Third IEEE Asia Pacific Conference on ASICs, the 1997, the 1999, the 2001 and the 2003 International Symposium on VLSI Technology, Systems, and Applications. He is a member of International Advisory Committee of the 2003 IEEE International Conference on Neural Networks and Signal Processing and has been a Member of the International Steering Committee of the IEEE Asia-Pacific Conference on Circuits and Systems since 2001. He was the Technical Program Chair of the 2003 Workshop on Consumer Electronics and the General Co-Chair of the First International Meeting on Microsensors and Microsystems in 2003, the General Chair of the 2004 IEEE Asia-Pacific Conference on Circuits and Systems. He is serving as the Meeting Co-Chair of the 9th International Workshop of Cellular Neural Networks and Their Applications in 2005, the Vice President-Region 10 of the IEEE Circuits and Systems (CAS) Society, a CAS Associate Editor of the *IEEE Circuits and Devices Magazine*, and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS.

Diana Marculescu (M'98) received the M.S. degree in computer science from Politehnica University of Bucharest, Romania, in 1991 and the Ph.D. degree in computer engineering from University of Southern California, Los Angeles, in 1998.

She is currently an Associate Professor of Electrical and Computer Engineering at Carnegie Mellon University, Pittsburgh, PA. Her research interests include energy aware computing, CAD tools for low power systems and emerging technologies (such as electronic textiles or ambient intelligent systems).

Dr. Marculescu is the recipient of a National Science Foundation Faculty Career Award (2000–2004), of an ACM-SIGDA Technical Leadership Award (2003), of the Carnegie Institute of Technology George Tallman Ladd Research Award (2004) and a Best Paper Award from IEEE Asia South-Pacific Design Automation COnference (ASPDAC 2005). She is an IEEE Circuits and Systems Society Distinguished Lecturer (2004–2005) and a Member of Executive Board of the ACM Special Interest Group on Design Automation (SIGDA).

Radu Marculescu (M'98) received the Ph.D. degree from the University of Southern California, Los Angeles, in 1998.

In 2000, he joined the electrical and computer engineering faculty of Carnegie Mellon University, Pittsburgh, PA, where he is currently an Assistant Professor. His research interests include SOC design methodologies, NOCs and fault tolerant communication, and ambient intelligent systems. He and his research group perform research on formal methods for SOC design of embedded applications. Of particular interest are fast methods for power and performance analysis that can guide the design process of portable information devices. Currently, the group develops novel approaches for exploiting concurrency and communication aspects in the design and optimization of complex heterogeneous applications.

Dr. Marculescu received the National Science Foundation's Career Award for the System-Level Power/Performance Analysis for Embedded Systems Design in 2001. He has recently received three Best Paper Awards in the area of systems design methodologies at the 2001 and 2003 editions of the Design and Test Conference in Europe (DATE), and 2003 edition of the Asia and South Pacific Design Automation Conference (ASP-DAC). He was also awarded the 2002 Ladd Research Award from Carnegie Institute of Technology.

Vijaykrishnan Narayanan received the B.E degree in computer science and engineering from the University of Madras, India, in 1993 and the Ph.D. degree in computer science and engineering from University of South Florida, Tampa, in 1998.

Since 1998, he has been with the Computer Science and Engineering Department, Pennsylvania State University, University Park, where he is currently an Associate Professor. His research interests are in the areas of energy-aware reliable systems embedded Java, nano/VLSI systems and computer architecture. He has authored and coauthored more than 100 papers in these areas. His current research projects are supported by National Science Foundation, DARPA/MARCO Gigascale Silicon Research Center, Office of Naval Research, Semiconductor Research Consortium and Pittsburgh Digital Greenhouse.

Dr. Narayanan has served as General Chair for the IEEE Computer Society Annual Symposium on VLSI in 2003 and as the Treasurer for the International Symposium on Low Power Electronics and Design since 2001. He also serves as the Vice-Chair for Student Activities for the IEEE Computer Society. He has received several awards including the IEEE CAS/VLSI Transactions Best Paper Award in 2002, the Penn State CSE Faculty Teaching Award in 2002, the ACM SIGDA outstanding new faculty award in 2000, Upsilon Pi Epsilon award for academic excellence in 1997, the IEEE Computer Society Richard E. Merwin Award in 1996, and the University of Madras first rank in Computer Science and Engineering in 1993.

Sani R. Nassif received the Ph.D. degree from Carnegie Mellon University, Pittsburgh, PA.

He worked for ten years at Bell Laboratories on various aspects of design and technology coupling including device modeling, parameter extraction, worst case analysis, design optimization, and circuit simulation. He joined the IBM Austin Research Laboratory, Austin, TX, in 1996, where he is presently managing the Tools and Technology Department, which is focuses on design/technology coupling, timing simulation and analysis, testing, low power design, and thermoelectric cooling.

Steven M. Nowick received the B.A. degree from Yale University, New Haven, CT, and the Ph.D. degree in computer science from Stanford University, Stanford, CA, in 1993.

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Dr. Nowick was a Co-Founder of the IEEE Async Symposia series, and has twice served as its Program Co-Chair in 1994 and 1999. He was also Program Chair of the 2002 IEEE/ACM International Workshop on Logic and Synthesis (IWLS). He has been a Member of several program committees, including the Design Automation Conference, the International Conference on Computer-Aided Design, the Design, Automation, and Test in Europe, the Async Symposium, the International Conference on Computer Design, TAU, the IWLS, and VLSI Design Conference. He is currently an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (since 2001). He received an National Science Foundation (NSF) Faculty Early Career (CAREER) Award in 1995, an Alfred P. Sloan Research Fellowship in 1995, and an NSF Research Initiation Award in 1993. He received Best Paper Awards at the 1991 IEEE International Conference on Computer Design and at the 2000 IEEE Async Symposium. He also received two medium-scale NSF Information Technology Research Awards in 2000.

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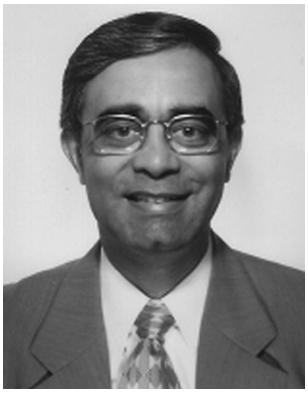
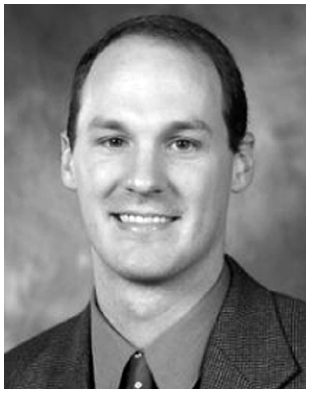
Dr. Sapatnekar has been an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING. He has served on the Technical Program Committee for various conferences, and as Technical Program and General Chair for the Tau workshop and for the International Symposium on Physical Design. He is currently a Distinguished Visitor for the IEEE Computer Society and has been a Distinguished Lecturer for the IEEE Circuits and Systems Society. He is a recipient of the NSF Career Award and Best Paper Awards at DAC 1997, ICCD 1998, DAC 2001, and DAC 2003.



Sunil Sherlekar received the B.Tech. degree in electrical engineering, the M.Tech. degree in computer science engineering, and the Ph.D. degree from Indian Institute of Technology (IIT) Bombay, Mumbai, India.

From 1982 to 1992, he was on the Faculty of Computer Science Engineering, IIT Bombay. From 1992 to 2002, he was with Sasken Communication Technologies, Bangalore, India, as their Chief Technology Officer. Since 2002, he has been with Tata Consultancy Services as the Head of their Centre of Excellence for Embedded Systems. He is also an Adjunct Professor with the Department of Electrical Engineering, IIT Bombay. His research interests are in the areas of VLSI design and testing, EDA, hardware description languages and optimal implementation of signal processing. He has published several papers in these areas and also a book (published by Kluwer Academic). He has been the Program Chair and General Chair for several IEEE-sponsored and other conferences. He is on the Steering Committee of the Asia and South Pacific Design Automation Conference. He is also on the Editorial Board of *Journal of Testing: Theory and Applications*.



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He worked at Hewlett-Packard Laboratories, Palo Alto, CA, from 1996 to 1998. After working as a Senior Research and Development Engineer in the Advanced Technology Group, Synopsys, Mountain View, CA, he is now an Assistant Professor of Electrical Engineering at the University of Michigan, Ann Arbor. He has published numerous papers in his field of research, which includes the modeling, characterization, and analysis of on-chip interconnect, advanced global signaling strategies, low-power circuit design techniques, and variability-aware circuit approaches.

Dr. Sylvester received a 2002 NSF CAREER award, the 2000 Beatrice Winner Award at ISSCC, two Outstanding Research Presentation Awards from the Semiconductor Research Corporation, and a Best Student Paper Award at the 1997 International Semiconductor Device Research Symposium. He is also the recipient of the 2003 Ruth and Joel Spira Outstanding Teaching Award. He is on the technical program committee of several design automation and circuit design conferences and was the general chair for the 2003 ACM/IEEE System-Level Interconnect Prediction (SLIP) Workshop. In addition, he is part of the International Technology Roadmap for Semiconductors (ITRS) U.S. Design Technology Working Group and made significant modeling contributions to the Design and System Drivers chapters of the 2001 ITRS. He is a member of ACM, American Society of Engineering Education, and Eta Kappa Nu.

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