Editorial

As I start my second two-year term (2017–2018) as the Editor-in-Chief (EIC) of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS (TVLSI), I wish the TVLSI readership a very happy new year and continued professional success. It gives me great pleasure to report on the state of the journal and our performance metrics. Over the past two years, TVLSI has seen a healthy increase in the number of submissions—from 687 in 2014 to 770 in 2015, and at the time of writing of this editorial, we are at 760 submissions for 2016. We expect the number of submissions for 2016 to cross 800 before the end of the year. TVLSI, therefore, continues to be the premier archival journal for university researchers and industry practitioners in the broad area of VLSI system design.

We have become increasingly selective to ensure high quality and our acceptance rate today stands at 31.6%. Our review cycle times have improved significantly and we take pride in providing authors with thorough reviews within two months of submission in most cases. For Regular Papers, our average time-to-decision for the first round of review is only 54 days. For Brief Papers, we provide a decision within 53 days on average. When revised manuscripts are also counted, our time-to-decision for Regular (Brief) papers in only 48 (46) days. This accomplishment has been made possible by the hard work of the Associate Editors. I thank them for their dedicated service, commitment to timeliness, and emphasis on quality for the papers that are recommended for publication. TVLSI is proud to have such an outstanding editorial board.

We have also taken steps to address the long-standing problem of publication backlog for TVLSI. When I started my EIC term, we were limited to an annual page budget of 2400 pages and papers were in the publication queue for nearly 1.5 years. While IEEE Xplore provides Early Access in a timely manner for accepted papers, it is nevertheless frustrating for authors to wait for so long to see their papers printed in hardcopy form. I am grateful to the IEEE for increasing our annual page budget to 3600 papers and our publication wait time is now down to six months. We are chipping away at this wait time, and we expect to soon be at a "steady-state" wait time of four months.

A benefit of the increase in page budget, and the reduced wait time to publication, is that we are now again publishing special sections on hot topics and emerging themes. This practice had to be discontinued during 2015–2016. We will publish two special sections in 2017 on Alternative Computing for Internet-of-Things (IoT) and Security in IoT, and we will continue to explore new themes for special sections in 2018.

I take this opportunity to thank the TVLSI steering committee for support and guidance. I am grateful to the steering committee members for the trust and confidence that they have placed in me. I am especially indebted to Associated EIC Massimo Alioto for being a tremendous source of support and for shouldering a major part of the leadership responsibilities of TVLSI. I also thank Stacey Weber Jackson for her immeasurable contributions to TVLSI as the journal administrator. As many of you know, Stacey has been with TVLSI for many years and she has worked with the past two EICs. She is my go-to-person on all TVLSI administrative matters, and she is a constant source of support for authors, reviewers, and Associate Editors. I applaud her dedication to TVLSI and thank her for her efforts in ensuring that the journal runs smoothly in every way.

As I start second my term, I would like to thank the members of the steering committee of TVLSI for their guidance and vision. I would also like to thank Joanna Gojlik, Heather McAlinn, Sonal Parikh, Katarzyna Pucilowska, Patrick Kempf, and all other staff members at the IEEE for their help in ensuring smooth journal operations.

Looking forward, TVLSI will continue to bring you in-depth research papers on the latest advances in VLSI systems, and respond in an agile manner to the convergence of emerging and mainstream technologies. To achieve this goal, I rely on your regular feedback, submission of articles, and active role as reviewers. I am excited by the opportunities that lie ahead in my second EIC term and I look forward to working with all of you.

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Krishnendu Chakrabarty (F'08) received the B.Tech. degree from the IIT Kharagpur, Kharagpur, India, in 1990, and the M.S.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, MI, USA, in 1992 and 1995, respectively.

He is currently the William H. Younger Distinguished Professor of Engineering with the Department of Electrical and Computer Engineering and a Professor of Computer Science at Duke University, Durham, NC, USA. He is also a Research Ambassador of the University of Bremen (Germany). His current research interests include testing and design-for-testability of integrated circuits, digital microfluidics, biochips, cyberphysical systems, optimization of enterprise systems, and smart manufacturing.

Dr. Chakrabarty is a Fellow of the ACM and a Golden Core Member of the IEEE Computer Society. He was a recipient of the Humboldt Research Award from the Alexander von Humboldt Foundation, Germany, the IEEE Computer Society Technical Achievement Award (2015), the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Donald O. Pederson Best Paper award (2015), and 12 best paper awards at major conferences. He received the Distinguished Alumnus Award from IIT Kharagpur in 2014. He is a Hans Fischer Senior Fellow (named after Nobel Laureate Prof. Hans Fischer) with the Institute for Advanced Study, Technical University of Munich, Munich, Germany. He has been an Invitational Fellow of the Japan Society for the Promotion of Sciences (JSPS), and held Visiting Professor positions at University of Tokyo and Nara Institute of Science and Technology in Japan. He has also been a Visiting Chair Professor at Tsinghua University in Beijing, China, and at National Cheng Kung University in Tainan, Taiwan. He served as the Editor-in-Chief of IEEE DESIGN & TEST from 2010 to 2012 and the *ACM Journal on Emerging Technologies in Computing Systems* from 2010 to 2015.

Massimo Alioto (M'01–SM'07–F'16) received the Laurea (M.Sc.) degree in electronics engineering and the Ph.D. degree in electrical engineering from the University of Catania, Catania, Italy, in 1997 and 2001, respectively.

In 2007, he was a Visiting Professor with École polytechnique fédérale de Lausanne, Lausanne, Switzerland. He was an Associate Professor with the Department of Information Engineering, University of Siena, Siena, Italy, and a Visiting Scientist with Intel Labs-CRL, Hillsboro, OR, USA, in 2013. From 2011 to 2012, he was a Visiting Professor with the University of Michigan, Ann Arbor, MI, USA. From 2009 to 2011, he was a Visiting Professor with the Berkeley Wireless Research Center, University of California at Berkeley, Berkeley, CA, USA. He has authored or co-authored over 220 publications on journals (80, mostly IEEE Transactions) and conference proceedings. He is a co-author of three books. He is currently an Associate Professor with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore, where he leads the Green IC group and the Integrated Circuits and Embedded Systems area. His current research interests include ultralow power VLSI circuits, self-powered and wireless nodes, near-threshold circuits for green computing, energy-quality scalable and widely energy-scalable VLSI circuits and systems, self-learning circuits for sensing and sensemaking, and circuit techniques for emerging technologies.

Dr. Alioto was the Chair of the VLSI Systems and Applications Technical Committee of the IEEE Circuits and Systems Society from 2010 to 2012, for which he was also a Distinguished Lecturer from 2009 to 2010, a member of the DLP Coordinating Committee (2011–2012), and a member of the Board of Governors (2015–2017). He served as a Guest Editor of several journal special issues, and also serves or has served as an Associate Editor of a number of IEEE and ACM journals. He is/was the Technical Program Chair of several conferences including the SOCC, ICECS, VARI, NEWCAS, ICM, PRIME, and a Track Chair including the ICCD, ISCAS, ICECS, VLSI-SoC, APCCAS, ICM.

Bevan M. Baas (SM'11) received the B.S. degree in electronic engineering from California Polytechnic State University, San Luis Obispo, CA, USA, in 1987, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1990 and 1999, respectively.

From 1987 to 1989, he was with Hewlett-Packard, Cupertino, CA. In 1999, he joined Atheros Communications, Santa Clara, CA, as an early employee and a core member of the team, which developed the first commercial IEEE 802.11a Wi-Fi wireless LAN solution. In 2003, he joined the Department of Electrical and Computer Engineering, University of California at Davis, Davis, CA, where he is currently a Professor. He leads projects in architectures, hardware, applications, and software tools for VLSI computation.

Dr. Baas was an NSF Fellow from 1990 to 1993 and a NASA GSR Fellow from 1993 to 1996. He received the National Science Foundation CAREER Award in 2006, the Best Paper Award at the ICCD 2011, the Best Student Paper Award third place at the IEEE Asilomar 2014, the Best Student Paper Award third place at the IEEE MWSCAS 2015, the WACIest Best-In-Session Paper at DAC 2010, and the Best Paper nominations at the IEEE Asilomar 2011 and the IEEE BioCAS 2010. He supervised the research that earned the College of Engineering Award for the Best Doctoral Dissertation Honorable Mention in 2013, and was awarded the Most Promising Engineer/Scientist Award by AISES in 2006. He is currently an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II. From 2007 to 2012 he was an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and he has served as a Guest Editor of Special Issues of IEEE MICRO and the *IEEE Design & Test of Computers*. He served as a Co-Chair of the HotChips 2011, a Track Co-Chair of the IEEE DSC 2017, Co-Chair of DAC PAPA Workshop 2011, and a Program Committee Member of numerous conferences.

Chirn Chye Boon (M'09–SM'10) received B.E. degree (Hons.) in electrical and the Ph.D. degree in electrical engineering from Nanyang Technological University (NTU), Singapore, in 2000 and 2004, respectively.

He was with Advanced RFIC, Singapore, where he was a Senior Engineer. Since 2005, he has been with NTU, where he is currently an Associate Professor. He specializes in the areas of radio frequency (RF) and MM-wave circuits and systems design for biomedical and communications applications. He has conceptualized, designed, and silicon-verified 80 circuits/chips for biomedical and communication applications. He has authored over 100 refereed publications in the fields of RF and MM-wave. He is an author of the book *Design of CMOS RF Integrated Circuits and Systems* (World Scientific Publishing).

Dr. Boon serves as a committee member for various conferences. He is currently an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS. He is the IEEE ELECTRON DEVICES LETTERS Golden Reviewer. He is the Program Director for RF and MM-wave research in the S50$million research center of excellence, VIRTUS (NTU) since 2010. He is the Principal Investigator for industry/government research grants of S$8,646,178.22. He is also one of the key NTU-team members of MIT-NTU joint collaboration Project Low Energy Electronic Systems, which has won the Singapore-MIT Alliance for Research and Technology International Research Grant proposal with a grant total of S$25million. He was a recipient of the Year-2 Teaching Excellence Award and the Commendation Award for Excellent Teaching Performance from the School of Electrical and Electronic Engineering, NTU.

Meng-Fan Chang (M'05–SM'14) received the M.S. degree from The Pennsylvania State University, State College, PA, USA, and the Ph.D. degree from the National Chiao Tung University, Hisnchu, Taiwan.

He is currently a Full Professor with National Tsing Hua University, Taiwan. He has worked in industry over 10 years. From 1996 to 1997, he designed memory compilers in Mentor Graphics, Warren, NJ, USA. From 1997 to 2001, he designed embedded SRAMs and flash in Design Service Division at TSMC, Hsinchu. From 2001 to 2006, he was a co-founder and the Director with the Intellectual Property Library Company, Hsinchu, where he developed embedded SRAM and ROM compilers, flash macros, and flat-cell ROM products. He is the co-author of numerous ISSCC, IEDM and VLSI Symposia papers. His current research interests include circuit designs for volatile and nonvolatile memory, ultra-low-voltage systems, 3D memory, circuit-device interactions, in-memory-computing, and memristor based neuromorphic computing.

Dr. Chang is currently an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION, IEEE TCAD and Institute of Electronics, Information, and Communication Engineers Electronics. He has been serving on technical program committees for ISSCC, IEDM, A-SSCC, ISCAS, VLSI-DAT, and numerous international conferences. He has been serving as the Associate Executive Director for Taiwan's National Program of Intelligent Electronics since 2011. He received the Academia Sinica (Taiwan) Junior Research Investigators Award in 2012, the Ta-You Wu Memorial Award of the National Science Council in 2011. He also received numerous awards from the Taiwan's National Chip Implementation Center, NTHU, MXIC Golden Silicon Awards, and ITRI.

Naehyuck Chang (F'12) received the B.S., M.S., and Ph.D. degrees from the Department of Control and Instrumentation, Seoul National University, Seoul, South Korea, in 1989, 1992, and 1996, respectively.

He was with the Department of Computer Science and Engineering, Seoul National University from 1997 to 2014. He was an LG Yonam Foundation Research Professor in 2005. He served as a Vice Dean of the College of Engineering with Seoul National University from 2011 to 2013. He has been a Full Professor with the Department of Electrical Engineering, South Korea Advanced Institute of Science and Technology, Daejeon, South Korea, since 2014. His current research interests include low-power embedded systems and design automation of things, such as systematic design and optimization of energy storage systems and electric vehicles.

Dr. Chang is a fellow of the Association for Computing Machinery (ACM) for his contributions to low-power systems. He received the 2014 ISLPED Best Paper Award, the 2011 SAE Vincent Bendix Automotive Electronics Engineering Award, the 2011 Sinyang Academic Award, the 2009 IEEE SSCS International SoC Design Conference Seoul Chapter Award, and several ISLPED Low-Power Design Contest Awards in 2002, 2003, 2004, 2007, 2012, and 2014. He is currently the Editor-In-Chief of the *ACM Transactions on Design Automation of Electronics Systems* and serves/served as an Associated Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION, IEEE TCAD, ACM TECS, IEEE ESL, IEEE TCAS-I, ACM TECS, and so on. He served for the ACM SIGDA (Special Interest Group on Design Automation) and is currently Past Chair of the ACM SIGDA. He was the TPC Co-Chair of the DAC 2016, ASP-DAC 2015, ICCD 2014, CODES+ISSS 2012, ISLPED 2009, and so on, and a General Co-Chair of the VLSI-SoC 2015, ICCD 2015 and 2014, ISLPED 2011, and so on.

Yao-Wen Chang (S'94–A'96–M'96–SM'12–F'13) received the B.S. degree from National Taiwan University (NTU), Taipei, Taiwan, in 1988, and the M.S. and Ph.D. degrees from the University of Texas at Austin, TX, USA, in 1993 and 1996, respectively, all in computer science.

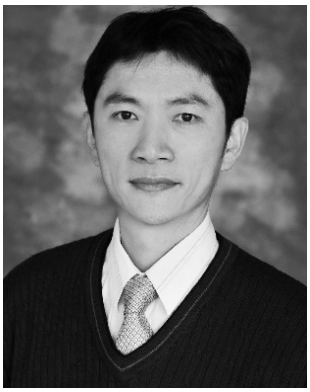
He is currently a Deputy Vice President of Academic Affairs of NTU and a Distinguished Professor of the Department of Electrical Engineering, NTU. He was an Associate Dean of the College of EECS from 2012 to 2016 and the Chairman of the Graduate Institute of Electronics Engineering from 2010 to 2013 of the same university. He was a Visiting Scholar with Massachusetts Institute of Technology, Cambridge, MA, USA, in 2014, and a Visiting Professor with Waseda University, Tokyo, Japan, from 2004 to 2010. He is a co-founder of the Maxeda Technology. He has co-edited one textbook on Electronic Design Automation and co-authored one book on routing and over 260 ACM/IEEE conference/journal papers in these areas, including highly cited works on floorplanning, placement, routing, design for manufacturability, and FPGA. His NTUplace3 placer was the core engine of the popular Digital Custom Placer of SpringSoft, acquired by the #1 EDA vendor, Synopsys, in 2012 for over $400 million U.S. His current research interests lie ininclude VLSI physical design and design for manufacturability/reliability.

Dr. Chang received four awards at the 50th ACM/IEEE DAC in 2013 for the 1st Most Papers in the 5th Decade (34 DAC papers in the 5th decade; #1 worldwide), and so on. He is a First Place winner of six recent major EDA Contests: the 2015 ACM ISPD Blockage-Aware Detailed Routing-Driven Placement Contest, the 2013 IEEE CAD Contest at ICCAD (Legalization and Detailed Placement), the 2012 ACM/IEEE DAC Routability-Driven Placement Contest, the 2012 ACM ISPD Discrete Gate Sizing Contest, the 2011 IEEE CEDA PATOS Timing Analysis Contest, and the 2009 ACM ISPD Clock Network Synthesis Contest. He has received 18 top-three contest awards during the past decade. He was a recipient of eight Best Paper Awards and the 2007 IEEE/ACM ICCAD Professor Margarida Jacome Memorial Award. He has received 23 Best Paper Award Nominations from top international conferences, including DAC (five times), ICCAD (four times), and ISPD (six times) since 2000. He has received many research awards, such as the Distinguished Research Awards (Highest Hons.) from the Ministry of Science and Technology of Taiwan (three times), and the IBM Faculty Awards (three times), the 2015 MXIC Chair Professorship, the 2009 Distinguished EE Professor from the CIEE, the 2004 MXIC Young Chair Professorship from the MXIC Corp, and Distinguished Teaching Award (Highest Hons. for top 1% teachers)/Excellent Teaching Awards (eight times). He is currently the IEEE CEDA Vice President of Conferences. He was an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS (TCAD) from 2008 to 2013. He is currently an Interview Editor of the IEEE DESIGN & TEST OF COMPUTERS. He has served as the steering committee/general/program chairs of the ISPD, the general/program chairs of the ICCAD, and a program chairs of the ASP-DAC and the FPT. He received an Outstanding Service Award from CEDA in 2015 and an ACM Service Award in 2012. He has served as the chair of the EDA Consortium of the Ministry of Education of Taiwan and an independent board director of Genesys Logic, Inc., a technical consultant of MediaTek Inc., RealTek Semiconductor Corp., and Faraday Technology Inc.

Chip-Hong Chang (S'92–M'98–M'03) received the B.Eng. degree (Hons.) from the National University of Singapore, Singapore, in 1989, and the M. Eng. and Ph.D. degrees from Nanyang Technological University (NTU), Singapore, in 1993 and 1998, respectively.

He served as a Technical Consultant in industry prior to joining the School of Electrical and Electronic Engineering (EEE), NTU, in 1999, where he is currently an Associate Professor. He holds joint appointments with the university as an Assistant Chair of Alumni with the School of EEE from 2008 to 2014, the Deputy Director of the Center for High Performance Embedded Systems from 2000 to 2011, and the Program Director of the Center for Integrated Circuits and Systems from 2003 to 2009. He has co-edited four books, authored ten book chapters and over 85 international journal papers, of which 54 are IEEE publications, and over 150 refereed international conference papers (mostly IEEE). His current research interests include hardware security and digital forensic, low-power and fault-tolerant computing, residue number systems, and application-specific digital signal processing.

Dr. Chang is a Fellow of the IET. He also served as an Advisor, a General Chair, a General Co-Chair, the Technical Program Co-chair, other organizing committee and technical program appointments for over 50 international conferences (mostly IEEE). He was the Editorial Advisory Board Member of the *Open Electrical and Electronic Engineering Journal* from 2007 to 2013 and *Journal of Electrical and Computer Engineering* from 2008 to 2014, and a Guest Editor of several journal special issues. He has been an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS since 2011, the IEEE ACCESS since 2013, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS and the IEEE TRANSACTIONS ON INFORMATION FORENSIC AND SECURITY since 2016, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I from 2010 to 2013, *Integration, the VLSI Journal* from 2013 to 2015, *Journal of Hardware and System Security* (Springer) since 2016 and *Microelectronics Journal* since 2014.



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Dr. Chang was the Executive Director of the National Program for Intelligent Electronics from 2011 to 2015 and the Director of the Taiwan integrated Circuit Design Society from 2013 to 2014. He was an Associate Editor of the *ACM Transaction on Design Automation of Electronic Systems*. He is currently an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER AIDED DESIGN.

Poki Chen (M'05) was born in Chiayi, Taiwan, in 1963. He received the B.S., M.S., and Ph.D. degrees from the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, in 1985, 1987 and 2001, respectively.

He was a Lecturer, an Assistant Professor, and an Associate Professor with the Department of Electronic Engineering, National Taiwan University of Science and Technology (NTUST), Taipei, from 1998 to 2011, where he is currently a Professor with the Department of Electronic and Computer Engineering. He was the Director of the System-on-Chip Research Center/Business Incubation Center, NTUST, since 2010. He current research interests include creating innovative analog applications for field-programmable gate array (FPGA) platforms, such as FPGA smart temperature sensor, FPGA digital-to-time, and time-to-digital converters, analog/mixed-signal integrated circuits and systems with an emphasis on time-domain signal processing circuits, such as time-domain smart temperature sensor, time-to-digital converter, digital pulse generator, digital pulse width modulator, and duty cycle corrector.

Dr. Chen serves on the Editorial Board of the International Scholarly Research Network Electronics. He is currently the Organizer of the IEEE International Conference on Intelligent Green Building and Smart Grid, and serves as the TPC Member and the Session Chair of various IEEE conferences, such as the International System-on-Chip Conference, the International Symposium on VLSI Design, Automation and Test, the International Future Energy Electronics Conference, Nordic Mediterranean Workshop on Time to Digital Converters, the International Symposium on Next-Generation Electronics, and the International Conference on Anti-Counterfeiting, Security and Identification. He currently serves as the Chair of the Department of Electronic and Computer Engineering, NTUST. He is currently an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS and the IEEE ACCESS.

Masud Chowdhury received the B.S. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, in 1999, and the Ph.D. degree in computer engineering from Northwestern University, Evanston, IL, USA, in 2004.

He was with University of Illinois at Chicago, Chicago, IL, the IBM Austin Research Lab, Austin, TX, USA and International Islamic University Chittagong, Chittagong, Bangladesh. He is currently an Associate Professor with the Department of Computer Science Electrical Engineering, University of Missouri-Kansas City (UMKC). He is in charge of the ECE Ph.D. Program at UMKC. He is the Director of the Micro and Nano Electronics Lab at UMKC. He is currently leading the effort to establish a new center, Center for Interdisciplinary Nano Technology Research with the School of Computing and Engineering, UMKC. He has authored over 130 articles in various journals and conferences in his fields of research, which includes micro and nanoelectronics and nanotechnology. His research has been funded by the U.S. Air Force, the NSF and the UM System internal grants. Mentoring students of diverse backgrounds and academic levels is one of the main focal points of his career. During his 11 years of faculty career he has supervised over 15 M.S. and Ph.D. Thesis students. He currently supervises ten Ph.D. and three M.S. Thesis students in his group at UMKC. He has been regularly supervising Undergraduate Research and High School students through different initiatives.

Dr. Chowdhury is currently serving as the Associate Editor of four leading journals in his field of research. He has completed his term as the Chair of the IEEE VLSI Systems and Applications Technical Committee. He has been serving in many conferences, symposiums, community outreach, and other professional committees in different capacities.

Pasquale Corsonello received the master's degree in electronics engineering from the University of Naples Federico II, Naples, Italy, in 1988.

He joined the Institute of Research on Parallel Computers, National Council of Research of Italy, Naples, where he was involved in the design and modeling of electronic transducers for high precision measurement, receiving a postgraduate two years grant. In 1992, he joined the Department of Electronics, Computer Science and Systems, University of Calabria, Rende, Italy, as a Research Associate. In 1997, he was appointed as an Assistant Professor of Electronics with the Department of Electronics Engineering and Applied Mathematics, Mediterranea University of Reggio Calabria, Reggio Calabria, Italy, where he also served as the Director of the Microelectronics Laboratory. In 2001, he was appointed as an Associate Professor of Electronics and the Chair of the Ph.D. Program in electronics engineering with the Mediterranea University of Reggio Calabria. In 2004, he was a Visiting Researcher with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY, USA. In 2005, he was appointed as an Adjunct Associate Professor with the Department of Electrical and Computer Engineering. He is currently an Associate Professor of Electronics with the Department of Informatics, Modeling, Electronics and System Engineering, University of Calabria. He has co-authored over 150 technical papers, and holds two patents in these fields. One of these papers is among the 25 most downloaded TVLSI papers in 2007. His current research interests include high-performance low-power CMOS design, VLSI architecture for image and video processing, and emerging nanoarchitectures.

Prof. Corsonello was a co-recipient of five Best Paper Awards. He has also received several grants from both private industries and government agencies for projects in these areas. He currently serves on the Technical Committees of several VLSI conferences, and as a Peer Reviewer for several VLSI journals. He is also an Associate Editor of the JOURNAL OF LOW POWER ELECTRONICS AND APPLICATIONS.

Ibrahim (Abe) M. Elfadel received the Ph.D. from MIT in 1993.

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Dr. Elfadel is a recipient of six Invention Achievement Awards, one Outstanding Technical Achievement Award, and one Research Division Award, all from IBM, for his contributions in the area of VLSI CAD. He is currently the Inventor or Co-Inventor of 50 issued U.S. patents with several others pending. He was the co-recipient of the 2014 D. O. Pederson Best Paper Award from the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN AUTOMATION FOR INTEGRATED CIRCUITS AND SYSTEMS. He is also the Co-Editor (with Prof. Gerhard Fettweis) of *3-D Stacked Chips: From Emerging Processes to Heterogeneous Systems*, Springer, 2016. From 2009 and 2013, he served as an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN. Since 2013 he has been serving on the Editorial Board of the *Microelectronics Journal* (Elsevier) and since 2014, he has been serving as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS. He has served on the Technical Program Committees of DAC, ICCAD, ASPDAC, DATE, ICCD, ICECS, and MWSCAS. He will be the General Co-chair of the IFIP/IEEE 25th International Conference on Very Large Scale Integration (VLSI-SoC), Abu Dhabi, 2017.

Said Hamdioui (M'99–SM'11) received the M.S.E.E. and Ph.D. degrees (Hons.) from the Delft University of Technology (TUDelft), Delft, The Netherlands, in 1997 and 2001, respectively.

He is currently leading Emerging Dependable Computing Technologies Research activities within the Computer Engineering Laboratory of TUDelft. He was with Intel Corporation, CA, USA, Philips Semiconductors Research and Development, Crolles, France, and Philips/NXP Semiconductors, Nijmegen, The Netherlands. He has authored one book and co-authored over 170 conference and journal papers. He has consulted for many companies such as Intel, STMicroelectronics, Altera, Atmel, Renesas, and Dialogue Semiconductors. He is strongly involved in the International Test Technology Community. He delivered dozens of keynote speeches, distinguished lectures, and invited presentations and tutorials at major international forums/conferences and leading semiconductor companies. His research focuses on two domains, such as dependable CMOS nano-computing, including reliability, testability, hardware security and emerging technologies and computing paradigms, including 3-D stacked ICs, memristors for logic and storage, in-memory-computing for big-data applications.

Dr. Hamdioui currently serves on the Editorial Board of the *Journal of Electronic Testing: Theory and Applications* and IEEE DESIGN & TEST. He is also a member of Association for European NanoElectronics Activities/European Nanoelectronics Initiative Advisory Council Scientific Committee Council.

Masanori Hashimoto (S'00–A'01–M'03–SM'11) received the B.E., M.E., and Ph.D. degrees from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively, all in communications and computer engineering.

Since 2016, he has been a Professor with the Department of Information Systems Engineering, Osaka University, Osaka, Japan. His current research interests include computer-aided design for digital integrated circuits, design for manufacturability and reliability, timing and power integrity analysis, and low-power circuit design.

Dr. Hashimoto was a recipient of the Best Paper Award at ASP-DAC 2004 and the Best Paper Award of *Institute of Electronics, Information, and Communication Engineers (IEICE) Transactions* in 2016. He is currently a Member of the Association for Computing Machinery, the Institute of Electronics, Information, and Communication Engineers (IEICE) and the Information Processing Society of Japan (IPSJ). He was on the technical program committees of international conferences including DAC, ICCAD, ASP-DAC, DATE, ISPD, ITC and Symposium on VLSI Circuits. He serves/served as an Associate Editor (AE) of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, an AE of *IEICE Transactions on Fundamentals* and an Associate Editor-in-Chief of *IPSJ Transactions on System LSI Design Methodology*.

Tsung-Yi Ho (SM'12) received the Ph.D. in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2005.

He is currently a Professor with the Department of Computer Science of the National Tsing Hua University, Hsinchu, Taiwan. He has presented 10 tutorials and contributed 10 special sessions in ACM/IEEE conferences, all in design automation for microfluidic biochips. His current research interests include design automation and test for microfluidic biochips and nanometer integrated circuits.

Dr. Ho has been a recipient of the Invitational Fellowship of the Japan Society for the Promotion of Science, the Humboldt Research Fellowship by the Alexander von Humboldt Foundation, and the Hans Fischer Fellow by the Institute of Advanced Study of the Technical University of Munich. He was a recipient of the Best Paper Awards at the VLSI Test Symposium (VTS) in 2013 and IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS in 2015. He served as a Distinguished Visitor of the IEEE Computer Society from 2013 to 2015, the Chair of the IEEE Computer Society Tainan Chapter from 2013 to 2015, and the Chair of the ACM SIGDA Taiwan Chapter from 2014 to 2015. He currently serves as an ACM Distinguished Speaker, a Distinguished Lecturer of the IEEE Circuits and Systems Society, and an Associate Editor of the *ACM Journal on Emerging Technologies in Computing Systems*, the *ACM Transactions on Design Automation of Electronic Systems*, IEEE sc Transactions on Computer-Aided Design of Integrated Circuits and Systems, and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, a Guest Editor of IEEE DESIGN & TEST OF COMPUTERS, and the Technical Program Committees of major conferences, including DAC, ICCAD, DATE, ASP-DAC, ISPD, and ICCD.

Houman Homayoun received the B.S. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 2003, the M.S. degree in computer engineering from the University of Victoria, Victoria, BC, Canada, in 2005, and the Ph.D. degree from the Department of Computer Science, University of California at Irvine, Irvine, CA, USA, in 2010.

He spent two years with the University of California at San Diego, La Jolla, CA, as National Science Foundation Computing Innovation Fellow awarded by the Computing Research Association and the Computing Community Consortium. He is currently an Assistant Professor of the Department of Electrical and Computer Engineering with the George Mason University (GMU), Fairfax, VA, USA. He also holds a joint appointment with the Department of Computer Science. He is the director of GMU's Green Computing and Heterogeneous Architectures Laboratory. His research interests include big data computing, heterogeneous computing, computer architecture, embedded system design, memory design, DRAM Design, and green and low power computing. His research projects have been funded by the National Science Foundation, the General Motors Company, the National Institute of Standards and Technology, and the Defense Advanced Research Projects Agency.

Dr. Homayoun served as a conference organizing committee member of GLSVLSI, ISPASS, GLOBECOM, and IEEE Big Data conferences. He was a recipient of the four-year Computer Science Department, University of California at Irvine, Chair Fellowship. He served as technical program committee member of several international conferences including ISPASS, DAC, DATE, CODES-ISSS, ICCD, GLSVLSI, IGSC, ISQED, ISLPED, and CF. He also organized several special sessions and tutorials on the topics of big data computing and heterogeneous architectures in DAC, DATE, and CODES-ISSS conferences. He received the Best Paper Award of the GLSVLSI 2016 conference. He is currently serving as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS.

Yuh-Shyan Hwang (M'04–SM'14) was born in Taipei, Taiwan, in 1966. He received the Ph.D. degree from the Department of Electrical Engineering, National Taiwan University, Taipei, in 1996.

He was a Lecturer with the Department of Electrical Engineering, Lee-Ming Institute of Technology, Taipei, from 1991 to 1996, and an Associate Professor with the Department of Electrical Engineering, Hwa Hsia University of Technology, Taipei, from 1996 to 2003. He joined the Department of Electronic Engineering, National Taipei University of Technology, Taipei, in 2003, where he is currently a Full Professor and serves as the Department Chair. He has authored over 100 international SCI journal and conference papers.

His current research interests include analog/power/mixed-signal integrated circuit design, VLSI design, current-mode analog signal processing, and integrated circuits for power management.

Dr. Hwang was a Technical Program Committee member of the VLSI Design/CAD Symposium in Taiwan from 2010 to 2015. He is a General Chair of 2017 IEEE International Conference on Consumer Electronics-Taiwan (ICCE-TW). He has served on the Editorial Board of the *Active and Passive Electronic Components* since 2010, the Editorial Board of the *Journal of Engineering* since 2012, and the Editorial Board of the *Far East Journal of Electronics and Communications*, and the *International Scholarly Research Notices* since 2013. He has served as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, and the IEEE ACCESS ONLINE OPEN ACCESS MEGA-JOURNAL since 2013. He has served as an Associate Editor of the IEEE Transactions on Circuits and Systems-II from 2014 to 2015. He has served as an Associate Editor of the *IET Electronics Letters* since 2016. He currently serves as a Reviewer for over ten technical journals.

Rajiv V. Joshi (F'02) received the B.Tech. degree from IIT Bombay, Mumbai, India, the M.S. degree from the Massachusetts Institute of Technology, Cambridge, MA, USA and the Dr.Eng.Sc. degree from Columbia University, New York, NY, USA.

He is currently a Research Staff Member with the Thomas J. Watson Research Center, IBM, Yorktown Heights, NY. His novel interconnects processes and structures for aluminum, tungsten and copper technologies are globally used till today for various technologies from sub-0.5 μm to 14 nm. He has led successfully pervasive statistical methodology for yield prediction and also the technology-driven SRAM with the IBM Server Group. He commercialized these techniques. He is an Industry Liaison for Princeton University, Princeton, NJ, USA, and Georgia Institute of Technology, Atlanta, GA, USA, as a part of the Semiconductor Research Corporation. He holds 58 invention plateaus and has over 215 U.S. patents and over 350 including international patents. He has authored and co-authored over 185 papers.

He is a WTN and ISQED Fellow and Distinguished Alumnus of IIT Bombay. He is a member of IBM Academy of technology. He is on the Board of Governors for the IEEE CAS. He received three Outstanding Technical Achievement, three highest Corporate Patent Portfolio Awards for licensing contributions. He received the best Associate Editor of TRANSACTIONS ON VERY LARGE SCALE INTEGRATION in 2016. He was a recipient of the 2015 BMM Award. He is inducted into New Jersey Inventor Hall of Fame in 2014 along with pioneer Nikola Tesla. He received the 2013 IEEE CAS Industrial Pioneer Award and the 2013 Mehboob Khan Award from Semiconductor Research Corporation. He is currently a Distinguished Lecturer of the IEEE CAS and the EDS society. He served on committees either as executive committee member/program chair or sub-committee chair of the IEEE ISLPED, IEEE VLSI design, IEEE CICC, IEEE International SOI conference, ISQED and AMC.

Tanay Karnik (M'88–SM'04–F'13) received the Ph.D. degree in computer engineering from the University of Illinois at Urbana-Champaign, Champaign, IL, USA.

He joined Intel Corporation, Hillsboro, OR, USA, in 1995. He is currently the Director of the University Research Office and a Principal Engineer with the Intel Labs, Hillsboro. He has presented several keynotes, invited talks and tutorials, and has served on six Ph.D. students' committees. He has authored over 80 technical papers, and has 55 issued and 28 pending patents. His current research interests include the areas of variation tolerance, power delivery, soft errors, and physical design.

Dr. Karnik is an International Symposium on Quality Electronic Design (ISQED) Fellow. He was a Member of the International Solid-State Circuits Conference, the Design Automation Conference, the International Conference on Computer-Aided Design, the International Conference on IC Design and Technology, and ISQED Program Committees, and the JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, the IEEE TRANSACTION ON VERY LARGE SCALE INTEGRATION, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I review committees. He received the Intel Achievement Award for the pioneering work on Integrated Power Delivery. He was the General Chair of the International Symposium on Low Power Electronics and Design in 2014, the Asia Symposium on Quality Electronic Design in 2010, the ISQED'09, the ISQED'08, and the International Conference on IC Design and Technology in 2008. He was a Guest Editor of the JOURNAL OF SOLID-STATE CIRCUITS. He is currently an Associate Editor of the IEEE TRANSACTION ON VERY LARGE SCALE INTEGRATION.

Mehran Mozaffari Kermani (S'00–M'11–SM'16) received the B.Sc. degree in electrical and computer engineering from the University of Tehran, Tehran, Iran, in 2005, and the M.E.Sc. and Ph.D. degrees from the Department of Electrical and Computer Engineering, University of Western Ontario, London, ON, Canada, in 2007 and 2011, respectively.

He joined the Advanced Micro Devices as a Senior ASIC/Layout Designer, integrating sophisticated security/cryptographic capabilities into accelerated processing. In 2012, he joined the Electrical Engineering Department, Princeton University, Princeton, NJ, USA, as a Natural Sciences and Engineering Research Council Post-Doctoral Research Fellow.

Dr. Kermani has been the TPC member for a number of conferences including HOST (Publications Chair), DAC, DATE, RFIDSec, LightSec, WAIFI, FDTC, and DFT. He was a recipient of the prestigious Natural Sciences and Engineering Research Council of Canada Post-Doctoral Research Fellowship in 2011 and the Texas Instruments Faculty Award (Douglas Harvey) in 2014. He was the lead Guest Editor of the IEEE/ACM TRANSACTIONS ON COMPUTATIONAL BIOLOGY AND BIOINFORMATICS and the IEEE TRANSACTIONS ON EMERGING TOPICS IN COMPUTING for special issues on security. He is currently an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, the *ACM Transactions on Embedded Computing Systems*, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, and the Guest Editor of the IEEE TRANSACTIONS ON DEPENDABLE AND SECURE COMPUTING for the special issue of Emerging Embedded and Cyber Physical System Security Challenges and Innovations (2016 and 2017).

Chulwoo Kim (S'98–M'02–SM'06) received the B.S. and M.S. degrees in electronics engineering from Korea University, Seoul, South Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Champaign, IL, USA, in 2001.

In 2001, he joined the IBM Microelectronics Division, Austin, TX, USA, where he was involved in cell processor design. Since 2002, he has been with the School of Electrical Engineering, South Korea University, Seoul, where he is currently a Professor. He has co-authored two books, namely, *CMOS Digital Integrated Circuits: Analysis and Design* (McGraw Hill, 4th edition 2014) and *High-Bandwidth Memory Interface* (Springer, 2013). His current research interests include wireline transceiver, memory, power management, and data converters.

Dr. Kim was a recipient of the Samsung HumanTech Thesis Contest Bronze Award in 1996, the ISLPED Low-Power Design Contest Award in 2001 and 2014, the DAC Student Design Contest Award in 2002, the SRC Inventor Recognition Award in 2002, the Young Scientist Award from the Ministry of Science and Technology of Korea in 2003, the Seoktop Award for excellence in teaching in 2006 and 2011, the ASP-DAC Best Design Award in 2008, the Special Feature Award in 2014, and the Korea Semiconductor Design Contest: Prime Minister Award in 2016. He served on the Technical Program Committee of the IEEE International Solid-State Circuits Conference and as a Guest Editor of the IEEE Journal of Solid-State Circuits. He was elected as the Distinguished Lecturer of the IEEE Solid-State Circuits Society for 2015âŁ“2016. He is currently on the Editorial Board of the IEEE Transactions on Vlsi Systems.

Tae-Hyoung Kim received the B.S. and M.S. degrees in electrical engineering from Korea University, Seoul, South Korea, in 1999 and 2001, respectively, the Ph.D. degree in electrical and computer engineering from the University of Minnesota, Minneapolis, MN, USA, in 2009.

From 2001 to 2005, he was with Samsung Electronics, where was involved in research on the design of high-speed SRAM memories, clock generators, and IO interface circuits. In 2007 and 2009, he was with IBM Thomas J. Watson Research Center, Yorktown Heights, NJ, USA, and the Broadcom Corporation, Irvine, CA, USA, where he performed research on circuit reliability, low power SRAM, and battery backed memory design, respectively. In 2009, he joined Nanyang Technological University, Singapore, as an Assistant Professor. He has authored/co-authored over 100 journal and conference papers and holds 17 U.S. and Korean patents registered. His current research interests include low power and high performance digital, mixed-mode, and memory circuit design, ultralow voltage circuits and systems design, variation and aging tolerant circuits and systems, and circuit techniques for 3-D ICs.

Dr. Kim has served numerous conferences as a committee member. He received the 2016 International Low Power Design Contest Award from ISLPED, a Best Paper Award at 2014 and 2011 ISOCC, the 2008 AMD/CICC Student Scholarship Award, the 2008 Departmental Research Fellowship from University of Minnesota, the 2008 DAC/ISSCC Student Design Contest Award, the 1999, 2001, and 2008 Samsung Humantec Thesis Award and, the 2005 ETRI Journal Paper of the Year Award. He is the Chair of the IEEE Solid-State Circuits Society Singapore Chapter. He serves as an Associate Editor of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS.

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From 2004 to 2005, he was a Design Engineer with Cypress Semiconductors, Bengaluru, and designed I/O circuits for micropower SRAMs. He joined the Circuit Research Lab, Intel Corporation, Hillsboro, OR, USA, in 2009, where he is currently a Staff Research Scientist. He has filed 30 patents and published 55 papers in referred journals and conferences. His current research interests include energy efficient integrated circuits and emerging nanotechnologies.

Dr. Kulkarni received the 2004 Best M.Tech. Student Award from IISc Bangalore, the 2008 SRC Inventor Recognition Awards, the 2008 ISLPED Design Contest Award, the 2008 Intel Foundation Ph.D. Fellowship Award, the 2008 SRC TECHCON Best Paper in Session Award, the 2010 Purdue School of ECE Outstanding Doctoral Dissertation Award, the 2015 IEEE Circuits and Systems Society's TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS Best Paper Award, and the 2015 Semiconductor Research Corporation's (SRC) Outstanding Industrial Liaison Award. He has participated in technical program committees of the A-SSCC, ISLPED, ISCAS, and ASQED conferences. He serves as an Associate Editor of the IEEE TRANSACTIONS ON VLSI SYSTEMS, and as an Industrial Liaison at the SRC, the STARnet, the Stanford System-X alliance, the Stanford-NMTRI Research Program.

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She served as a Program Director of the Research and Innovation with J. P. Morgan and Research Program Manager/Executive Staff to CIO at IBM Corporate Headquarters, North Castle, NY. She is currently a Researcher, the Executive Director and an Adjunct Professor with Columbia University, New York, NY, USA.

Dr. Kursun received a number of IBM Outstanding Research and Technical Accomplishment Awards and the Invention and High-Value Patent Awards for her research work. She received the Best Paper Award at the IEEE International Symposium on Low Power Design and the IEEE International Conference in computer design. He is currently serving as an Associate Editor of the IEEE TRANSACTIONS ON EMERGING TECHNOLOGIES IN COMPUTING, *ACM Journal on Emerging Technologies in Computing* and the IEEE TRANSACTIONS ON COMPUTERS, and the IEEE TC.

Erik Larsson received the M.Sc., the Licentiate of Engineering and the Ph.D degrees from Linköping University, Sweden, in 1994, 1998 and 2000, respectively.

From 2001 to 2002, a scholarship from Japan Society for the Promotion of Science supported a Post-Doctoral with the Nara Institute of Science and Technology, Japan. From 2003 to 2011, he was with Linköping University as an Assistant Professor from 2003 to 2005 and as an Associate Professor from 2006 to 2011. He received scholarship from the Swedish Foundation for Strategic Research for a sabbatical with NXP Semiconductors, The Netherlands, from 2008 to 2010. He is currently an Associate Professor (Docent) with the Department of Electrical and Information Technology at Lund University, Sweden. He authored the book *Introduction to Advanced System-on-Chip Test Design and Optimization* (Springer 2005). His current research interests include test planning for manufacturing test, test during operation (*insitu*), scan-chain diagnosis, silicon debug and validation, stacked 3-D chip test, fault-tolerance for multiprocessor system-on-chip (MPSoCs), and property checking in distributed systems (MPSOcS with network-on-chip). He has more than 140 publications in these areas.

Dr. Larsson received the Institution of Engineering and Technology Premium Award, 2009, and the Best Paper Award at the IEEE European Test Symposium, 2016, and the IEEE Asian Test Symposium, 2002. He supervised the thesis that won prize as a Best Master Thesis in engineering in Sweden (Lilla Polhemspriset 2008). He has served/serving for major conferences such as the ITC, DATE, VLSI Design, VTS, ETS, ATS, VLSI-SOC, GLSVLSI, and DDECS. He was a Vice Program Chair of the ETS in 2010, the Program Chair for the ETS in 2011, and a Topic Chair at the DATE, ETS, VLSI Design, and GLSVLSI.

Hai (Helen) Li (M'08–SM'16) received the B.S. and M.S. degrees in microelectronics from Tsinghua University, Beijing, China, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA, in 2004.

She is currently an Associate Professor with the Department of Electrical and Computer Engineering at Duke University, Durham, NC, USA. She was with Qualcomm Inc., San Diego, CA, USA, Intel Corporation, Santa Clara, CA, Seagate Technology, Bloomington, MN, USA, the Polytechnic Institute of New York University, Brooklyn, NY, USA, and the University of Pittsburgh, Pittsburgh, PA, USA. She has authored or co-authored over 170 technical papers published in peer-reviewed journals and conferences and holds 76 granted U.S. patents. She authored a book entitled *Nonvolatile Memory Design: Magnetic, Resistive, and Phase Changing* (CRC Press, 2011). Her current research interests include memory design and architecture, neuromorphic architecture for brain-inspired computing systems, and architecture/circuit/device cross-layer optimization for low power and high performance.

Dr. Li received five Best Paper Awards and seven Best Paper Nominations from ISQED, ISLPED, DATE, ISVLSI, ASPDAC, ICCAD, and DAC. She serves as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, the *ACM Transactions on Design Automation of Electronic Systems*, the IEEE TRANSACTIONS ON MULTI-SCALE COMPUTING SYSTEMS, the IEEE TRANSACTIONS ON COMPUTER AIDED DESIGN, and the *IET Cyber-Physical Systems: Theory & Applications*. She has served as technical program committee members for over 20 international conference series. She was a recipient of the NSF CAREER Award in 2012 and the DARPA YFA Award in 2013.

Huawei Li (M'00–SM'09) received the B.S. degree in computer science from Xiangtan University, Hunan, China, in 1996, and the M.S. and Ph.D. degrees from the Institute of Computing Technology (ICT), Chinese Academy of Sciences (CAS), Beijing, China, in 1999 and 2001, respectively.

She visited the University of California at Santa Barbara, Santa Barbara, CA, USA, from 2009 to 2010. She has been a Professor with ICT, CAS, since 2008. She has authored over 160 technical papers, and holds 20 Chinese patents. Her current research interests include testing of VLSI/SOC circuits, design verification, design for reliability, fault tolerance, and approximate computing.

Dr. Li has been on the Editorial Board of the *Journal of Computer-Aided Design and Computer Graphics* (in Chinese) since 2011, and on the Editorial Board of the JOURNAL OF COMPUTER RESEARCH AND DEVELOPMENT (in Chinese) since 2014. She was a recipient of the 2012 National Technology Invention Award of China. She was the Technical Program Co-Chair of the IEEE Asian Test Symposium in 2007 and the General Co-Chair in 2014. She was the Technical Program Chair of the IEEE Workshop on RTL and High Level Testing (WRTLT) in 2003 and the Technical Program Vice-Chair in 2013. She has served as the Steering Committee Chair of WRTLT (2014–2016), served as the Secretary General (2008–2015) and the Chair (since 2016) of the China Computer Federation Technical Committee on Fault-Tolerant Computing, and served on the technical program committees for several IEEE conferences. She has been an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION since 2015.

Patrick Mercier received the B.Sc. degree from the University of Alberta, Canada, in 2006, and the S.M. and Ph.D. degrees from Massachusetts Institute of Technology, Cambridge, MA, USA, in 2008 and 2012, respectively.

He is currently an Assistant Professor of the Electrical and Computer Engineering and a Co-Founder/Co-Director of the Center for Wearable Sensors at University of California at San Diego (UCSD), La Jolla, CA, USA. He has co-edited two books: *Power Management Integrated Circuits* (CRC Press, 2016), and *Ultra-Low-Power Short-Range Radios* (Springer, 2015). His current research interests include the design of energy-efficient mixed-signal systems, RF circuits, power converters, and sensor interfaces for wearable, medical, and mobile applications.

Dr. Mercier has received numerous awards, including the UCSD Academic Senate Distinguished Teaching Award in 2016, the DARPA Young Faculty Award in 2015, the Beckman Young Investigator Award in 2015, and the International Solid-State Circuits Conference (ISSCC) Jack Kilby Award in 2010. He is currently an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and the IEEE TRANSACTIONS ON VLSI.

Prabhat Mishra (M'04–SM'08) received the Ph.D. degree in computer science and engineering from the University of California at Irvine, Irvine, CA, USA, in 2004.

He spent several years in various companies including Intel, Motorola, Synopsys and Texas Instruments. He is currently a Professor with the Department of Computer and Information Science and Engineering (CISE), University of Florida (UF), Gainesville, FL, USA, where he leads the CISE Embedded Systems Lab. He has authored five books and over 125 research articles in premier international journals and conferences. His current research interests include design automation of embedded systems, energy-aware computing, reconfigurable architectures, hardware security and trust, system validation and verification, and post-silicon debug.

Dr. Mishra's research has been recognized by several awards including the NSF CAREER Award from the National Science Foundation, IBM Faculty Award, three best paper awards (ISQED 2016, VLSI Design 2011, and CODES+ISSS 2003), and EDAA Outstanding Dissertation Award from the European Design Automation Association. He currently serves as the Deputy Editor-in-Chief of the *IET Computers & Digital Techniques*, and as an Associate Editor of the *ACM Transactions on Design Automation of Electronic Systems*, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and the *Journal of Electronic Testing*. He has served on many organizing committees and technical program committees of premier ACM and IEEE conferences. He is currently serving as an ACM Distinguished Speaker. He is an ACM Distinguished Scientist.

Makoto Nagata received the B.S. and M.S. degrees in physics from Gakushuin University, Tokyo, Japan, in 1991 and 1993, respectively, and the Ph.D. degree in electronics engineering from Hiroshima University, Higashihiroshima, Japan, in 2001.

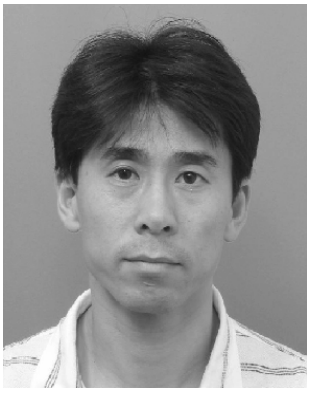
He was a Research Associate with Hiroshima University from 1994 to 2002, and an Associate Professor of Kobe University, Kobe, Japan, from 2002 to 2009. He is currently a Professor of the Graduate School of Science, Technology and Innovation, Kobe University. His current research interests include design techniques toward high performance mixed analog, RF, and digital VLSI systems with particular emphasis on power/signal/substrate integrity and electromagnetic compatibility, testing and diagnosis, 3-D system integration, and connectivity and security applications.

Dr. Nagata has been a member of a variety of technical program committees of international conferences such as the Symposium on VLSI Circuits (2002–2009), the Custom Integrated Circuits Conference (2007–2009), the Asian Solid-State Circuits Conference (2005–2009), and the International Solid-State Circuits Conference (2014–). He was a co-recipient of the Best Paper Award from the 3D-Test 2013, the CHES 2014, and the APEMC 2015. He was a Technical Program Chair (2010–2011) and a Symposium Chair (2012–2013) for Symposium on VLSI circuits. He also served as an Associate Editor of the *Institute of Electronics, Information, and Communication Engineers Transactions on Electronics* (2002–2005). He is currently an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS (2015–), and also a Chair of the IEEE SSCS Kansai Chapter (2017).

Arun S. Natarajan received the B.Tech. degree from IIT Madras, Chennai, India, in 2001, and the M.S. and Ph.D. degrees from the California Institute of Technology, Pasadena, CA, USA, in 2003 and 2007, respectively, all in electrical engineering.

From 2007 to 2012, he was a Research Staff Member of the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA, where he was involved in millimeter-wave (mm-wave) phased arrays for multiGb/s data links and airborne radar and on self-healing circuits for increased yield in submicron process technologies. In 2012, he joined Oregon State University, Corvallis, OR, USA, as an Assistant Professor with the School of Electrical Engineering and Computer Science. His current research interests include RF, mm-wave and submm-wave integrated circuits, and systems for high-speed wireless communication and imaging.

Dr. Natarajan was a recipient of the National Talent Search Scholarship from the Government of India (1995–2000), the Caltech Atwood Fellowship in 2001, the IBM Research Fellowship in 2005, the 2011 Pat Goldberg Memorial Award for the best paper in computer science, electrical engineering, and mathematics published by IBM Research, the CDADIC Best Faculty Project Award in 2014 and 2016, the NSF CAREER award in 2016, and the Oregon State University Engelbrecht Young Faculty Award in 2016. He serves on the Technical Program Committee of the IEEE International Solid-State Circuits Conference, the IEEE Radio-Frequency Integrated Circuits Conference and is also an Associate Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.



Koji Nii received the B.E. and M.E. degrees in electrical engineering from Tokushima University, Tokushima, Japan, in 1988 and 1990, respectively, and the Ph.D. degree in informatics and electronics engineering from Kobe University, Hyogo, Japan, in 2008.

In 1990, he joined the ASIC Design Engineering Center, Mitsubishi Electric Corporation, Itami, Japan, where he was involved in designing 0.8 um to 130 nm embedded SRAMs and CAMs for CMOS ASICs, and researching on SOI SRAM development. In 2003, he was transferred to Renesas Technology Corporation, Itami, Japan, which is a joint company of Mitsubishi Electric Corporation and Hitachi Ltd., in the semiconductor field. He has been working on designing 45 nm to 90 nm embedded low-power and high-speed SRAM macros, and researching on the 45 nm SRAM assist circuits techniques to enhance the functional margin against variations. He transferred his work location from Itami, Hyogo, to Kodaira, Tokyo, in 2009, where he has been working on designing and researching on 28 nm High-k/Metal-gate and 16 nm FinFET SRAM macros. His current responsibility is Department Manager. He currently works on the research and development of embedded SRAM/TCAM/ROM and low-power design techniques with power gating in advanced technology nodes (28, 16, and 10 nm and beyond) with the 1st Solution Business Unit, Renesas Electronics Corporation, Kodaira, Tokyo, Japan. He is also a Visiting Professor of Graduate School of Natural Science and Technology, Kanazawa University, Ishikawa, Japan. He holds 90 U.S. patents, and has authored 32 IEEE/IEICE papers and 76 talks at major international conferences.

Dr. Nii is a senior member of the IEEE Solid-State Circuits Society, IEEE Computer Society and the IEEE Electron Devices Society. He is a member of the Institute of Electronics, Information and Communication Engineers, Japan. He received the Best Paper Award at the IEEE International Conference on Microelectronic Test Structures in 2007 and IEEE International Symposium on Quality Electronic Design in 2013. He also received the LSI IP Design Award in 2007 and 2008, Japan. He is a Technical Program Committee of the IEEE CICC and the IEEE IEDM and an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS.

Partha Pratim Pande received the M.S. degree in computer science from the National University of Singapore, Singapore, and the Ph.D. degree in electrical and computer engineering from the University of British Columbia, Vancouver, BC, Canada.

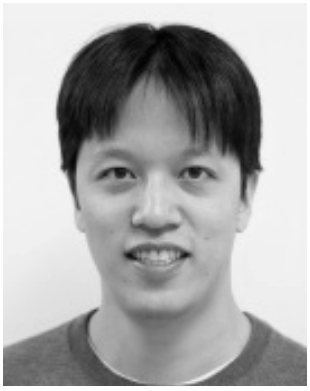
He is currently a Professor and Holder of the Boeing Centennial Chair in computer engineering with the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA, USA. His current research interests include novel interconnect architectures for multicore chips, on-chip wireless communication networks, and hardware accelerators for biocomputing.

Dr. Pande serves on the Editorial Boards of *ACM Journal of Emerging Technologies in Computing Systems*, and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS and *Sustainable Computing: Informatics and Systems*. He has won the NSF CAREER Award in 2009. He is the Winner of the Anjan Bose Outstanding Researcher Award from the College of Engineering, Washington State University, in 2013. He serves with the Program Committees of many reputed international conferences. He is the TPC chair of the IEEE Network-on-Chip Symposium 2015. He was the TPC chair of the IEEE Green Computing Conference (IGCC) in 2014 and the General Chair of IGCC 2015. He is currently the Editor-in-Chief (EIC) of the IEEE TRANSACTIONS ON MULTISCALE COMPUTING SYSTEMS, and an Associate EIC of the IEEE DESIGN & TEST.

Ioannis Savidis received the B.S.E. degree in electrical and computer engineering and biomedical engineering from Duke University, Durham, NC, in 2005, and the M.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Rochester, Rochester, NY, USA, in 2007 and 2013, respectively.

He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA, USA, where he directs the Integrated Circuits and Electronics Design and Analysis Laboratory. He has held visiting research positions with the 3-D Integration Group, Freescale Semiconductor, Austin, TX, USA, in 2007, and with the System on Package and 3-D Integration Group, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, in 2008, 2009, 2010, and 2011. His current research and teaching interests include analysis, modeling, and design methodologies for high-performance digital and mixed-signal integrated circuits, power management for system-on-chip and microprocessor circuits, including on-chip dc-dc converters, emerging integrated circuit technologies, IC design for trust (hardware security), and interconnect related issues in 2-D and 3-D ICs. He has authored or co-authored over 40 technical papers published in peer-reviewed journals and conferences, and holds 4 pending patents.

Dr. Savidis is a member on the Editorial Boards of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, the *Microelectronics Journal*, and the *Journal of Circuits, Systems and Computers*. He serves on the organizing committees and technical program committees of many international conferences, including the IEEE International Symposium on Circuits and Systems, the Great Lakes Symposium on Very Large Scale Integration, the ACM/IEEE System Level Interconnect Prediction Workshop, and the IEEE International Symposium on Hardware Oriented Security and Trust.



Mingoo Seok received the B.S. (*summa cum laude*) degree in electrical engineering from Seoul National University, Seoul, South Korea, in 2005, and the M.S. and Ph.D. degrees from the University of Michigan, Ann Arbor, MI, USA, in 2007 and 2011, respectively, all in electrical engineering.

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Dr. Tan is serving (or has served) on Technical Program Committee of the DAC, ICCAD, DATE, ISLPED, ASPDAC, ICCD, ISQED, SMACD, ASICON, ICSICT, FAC and the ACM/SIGDA Outstanding PhD Dissertation Award Selection Committee and IEEE Technical Committee on Cyber-Physical System. He received the Outstanding Oversea Investigator Award from the National Natural Science Foundation of China in 2008. He received the NSF CAREER Award in 2004. He received the Best Paper Award from the 2007 IEEE International Conference on Computer Design, the Best Paper Award from the 1999 IEEE/ACM Design Automation Conference, and Best Paper Award Nomination from the IEEE/ACM Design Automation Conferences in 2005, 2009, and 2014, and one Best Paper Award Nomination from ASPDAC in 2015. He now is serving as the Editor-In-Chief of *Integration, The VLSI Journal*. He is also serving as an Associate Editor for three journals: the IEEE TRANSACTION ON VERY LARGE SCALE INTEGRATION SYSTEMS, the *ACM Transaction on Design Automation of Electronic Systems*.

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Dr. Tehranipoor is a Golden Core Member of IEEE, Member of ACM, and ACM SIGDA. He was a recipient of several best paper awards and the 2008 IEEE Computer Society (CS) Meritorious Service Award, the 2012 IEEE CS Outstanding Contribution, the 2009 NSF CAREER Award, and the 2014 MURI award. He currently serves on the program committee of over a dozen of leading conferences and workshops. He served as Program Chair of the 2007 IEEE Defect-Based Testing workshop, Program Chair of the 2008 IEEE Defect and Data Driven Testing (D3T) workshop, a Co-Program Chair of the 2008 International Symposium on Defect and Fault Tolerance in VLSI Systems (DFTS), a General Chair of the D3T-2009 and the DFTS-2009, and a Vice-General Chair of the NATW-2011. He co-founded the IEEE International Symposium on Hardware-Oriented Security and Trust (HOST) and served as the HOST-2008 and the HOST-2009 General Chair. He is currently serving as an Associate Editor for JETTA, JOLPE, IEEE TVLSI and *ACM Transaction on Design Automation of Electronic Systems*. Dr. Tehranipoor served as the Founding Director for CHASE and CSI centers with the University of Connecticut. He is currently serving as Co-Director of the Florida Institute for Cybersecurity Research.

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He has authored 28 benchmark suites with over 1,100 boolean satisfiability (SAT) formulas that have been used widely in research on SAT solvers for the last 15 years, including the annual SAT-solver competitions and in hundreds of papers on SAT solving, and have had a significant impact on the field of SAT that has applications to solving many VLSI problems. His research is on formal verification of hardware and software, SAT, and solving of constraint satisfaction problems and combinatorial problems by efficient translation to SAT.

Dr. Velev is an ACM Distinguished Member/Distinguished Scientist, and Senior Member of AIAA and AAAI. For his Ph.D. research on automatic formal verification of pipelined processors, Miroslav received the EDAA Outstanding Dissertation Award. He is the Founder and President of Aries Design Automation, a company that develops formal verification and related technologies for NASA, the National Institute of Standards and Technology, the Department of Defense, and the Department of Energy.

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Dr. Wen was a recipient of the Institute of Electronics, Information, and Communication Engineers-ISS Best Paper Award in 2008. He is the co-chair of the Technical Activity Committee on Power-Aware Testing, Test Technology Technical Council, Computer Society, IEEE. He has been an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS since 2012.

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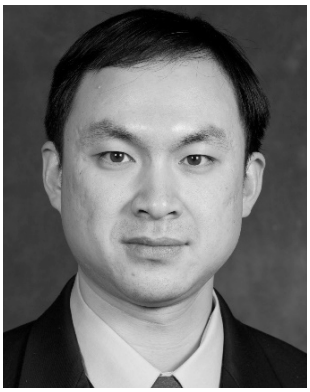

Zhengya Zhang received the B.A.Sc. degree in computer engineering from the University of Waterloo, Waterloo, ON, Canada, in 2003, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley, Berkeley, CA, USA, in 2005 and 2009, respectively.

He has been with the faculty at the University of Michigan, Ann Arbor, MI, USA, since 2009, where he is currently an Associate Professor with the Department of Electrical Engineering and Computer Science. His current research interests include low-power and high-performance VLSI circuits and systems for computing, communications, and signal processing.

Dr. Zhang was a recipient of the National Science Foundation CAREER Award in 2011, the Intel Early Career Faculty Award in 2013, the David J. Sakrison Memorial Prize for outstanding doctoral research in electrical engineering and computer sciences from UC Berkeley, and the Best Student Paper Award at the Symposium on VLSI Circuits. He serves as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS since 2015. He was also an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS from 2013 to 2015, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS from 2014 to 2015.

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