Editorial

WELCOME to the first issue of the IEEE TRANSACTIONS ON VLSI SYSTEMS (TVLSI) for 2015. It is my pleasure to write to you as the new Editor-in-Chief (EIC) of TVLSI. I am honored to succeed Prof. Yehea Ismail and continue the tradition of excellence established by him and the EICs before him. I take this opportunity to thank Yehea for his dedicated service and for setting high standards for the journal. Under the visionary leadership of the past EICs, TVLSI is now firmly established as the premier archival journal for university researchers and industry practitioners in the broad area of VLSI system design. My association with TVLSI goes back all the way to my days as a graduate student; my first journal paper was published in TVLSI over 20 years ago, and since then I have been proud to publish some of my best works here. I served as an Associate Editor (AE) for TVLSI during 2005–2009 and as a member of its steering committee during the past two years. I am therefore especially delighted to contribute to the journal as EIC and continue my long association with it.

I take this opportunity to welcome the members of the new editorial board. Some of the AEs from the previous editorial board will continue to serve the journal, but a majority of AEs will start new terms. The AEs are active and respected researchers in their fields, and they span a wide range of topics covered by TVLSI. One of my objectives in forming the editorial board was to rejuvenate it with new members and to replace AEs who have served the journal for two or more terms. I thank the outgoing AEs for their dedicated service to the journal. The new editorial board reflects a healthy balance between participation from academia and industry. In addition, the AEs represent all the major geographical regions that make up the TVLSI community. The biographies and photographs of the AEs in the new editorial board are provided. The AEs are also listed in the journal's inside cover.

I am happy to announce that Prof. Massimo Alioto from the National University of Singapore will continue as the Associate Editor-in-Chief of TVLSI. Massimo has served TVLSI with distinction over the past many years, and he is a highly respected researcher in the field. He will continue to lead our efforts to ensure timely and high-quality reviews for papers submitted to TVLSI. We will work to reduce the time that it currently takes for authors to get decisions on their submissions. Massimo and I will also work with the TVLSI steering committee to address the pressing problem of an excessively long backlog of articles that are queued for publication. We are committed to reducing the time to publication for accepted papers and I promise authors that we will do everything possible to resolve this problem.

I am delighted that Ms. Stacey Weber Jackson will continue as the TVLSI Editorial Assistant. As many of you know, Stacey has been with TVLSI for many years now, and she has worked with the past two EICs. I applaud her dedication to TVLSI and thank her for her efforts in ensuring that the journal runs smoothly in every way. I look forward to working closely with Stacey during my EIC term.

As I start my term, I would like to thank the members of the steering committee of TVLSI for their guidance and vision. I would also like to thank Mr. William Colacchio, Ms. Joanna Gojlik, Ms. Sonal Parikh, Ms. Katarzyna Pucilowska, and all other staff members at the IEEE for their help in ensuring smooth journal operations.

Looking forward, TVLSI will continue to bring you in-depth research papers on the latest advances in VLSI systems, and respond in an agile manner to the convergence of emerging and mainstream technologies in areas such as energy systems, hardware trust and design for secure systems, circuit/system design methods for nanotechnologies, neuromorphic systems, and bio-inspired computing. To achieve this goal, I rely on your regular feedback, submission of articles, and active role as reviewers. TVLSI will continue to maintain a vibrant editorial board consisting of active and visionary researchers. Existing partnerships with conferences and professional communities will be strengthened, and new partnerships will be created to reach out to a wider audience. I am excited by the opportunities that lie ahead and I look forward to working with all of you.

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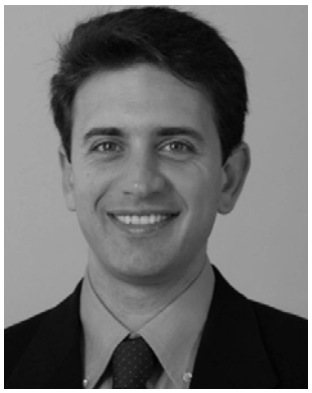
Krishnendu Chakrabarty (F'08) received the B.Tech. degree from IIT Kharagpur, Kharagpur, India, in 1990, and the M.S.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, MI, USA, in 1992 and 1995, respectively.

He is currently the William H. Younger Distinguished Professor of Engineering with the Department of Electrical and Computer Engineering and a Professor of Computer Science at Duke University, Durham, NC, USA. He serves as the Executive Director of Graduate Studies in Electrical and Computer Engineering. He has authored 16 books on these topics (with one more book in press), published over 500 papers in journals and refereed conference proceedings, and given over 220 invited, keynote, and plenary talks. He has also presented 40 tutorials at major international conferences. His current research interests include testing and design-for-testability of integrated circuits, digital microfluidics, biochips, and cyberphysical systems, and optimization of digital print and enterprise systems. He has also led major research projects in the past on wireless sensor networks, embedded real-time operating systems, and chip cooling using digital microfluidics.

Prof. Chakrabarty is a fellow of Association for Computing Machinery (ACM), and a Golden Core Member of the IEEE Computer Society. He holds five U.S. patents, with several patents pending. He was a 2009 Invitational Fellow of the Japan Society for the Promotion of Science. He was a recipient of the 2008 Duke University Graduate School Dean's Award for excellence in mentoring, and the 2010 Capers and Marion McDonald Award for Excellence in Mentoring and Advising, Pratt School of Engineering, Duke University. He served as a Distinguished Visitor with the IEEE Computer Society from 2005 to 2007 and 2010 to 2012, and as a Distinguished Lecturer with the IEEE Circuits and Systems Society from 2006 to 2007 and 2012 to 2013. He is currently an ACM Distinguished Speaker. He was a recipient of the National Science Foundation Early Faculty (CAREER) Award, the Office of Naval Research Young Investigator Award, the Humboldt Research Award from the Alexander von Humboldt Foundation, Germany, and 10 Best Paper Awards at the major IEEE conferences, Distinguished Alumnus Award from IIT Kharagpur. He served as the Editor-in-Chief of the IEEE DESIGN AND TEST OF COMPUTERS from 2010 to 2012. He serves as the Editor-in-Chief of the *ACM Journal on Emerging Technologies in Computing Systems* and he will serve as the Editor-in-Chief of the IEEE TRANSACTIONS ON VLSI SYSTEMS in 2015. He is also an Associate Editor of the IEEE TRANSACTIONS ON COMPUTERS, the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and the *ACM Transactions on Design Automation of Electronic Systems*. He serves on the Steering Committee of the IEEE TRANSACTIONS ON VLSI SYSTEMS and the IEEE JOURNAL ON EXPLORATORY SOLID-STATE COMPUTATIONAL DEVICES AND CIRCUITS, and as an Editor of the *Journal of Electronic Testing: Theory and Applications*. He was an Associate Editor of the IEEE TRANSACTIONS ON VLSI SYSTEMS from 2005 to 2009, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS from 2001 to 2013, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 2005 to 2006, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2010 to 2013.



Massimo Alioto (M'01–SM'07) received the M.Sc. degree in electronics engineering and the Ph.D. degree in electrical engineering from the University of Catania, Catania, Italy, in 1997 and 2001, respectively.

He was an Associate Professor with the University of Siena, Siena, Italy, and a Visiting Scientist with the Intel Labs-Circuits Research Laboratory, Hillsboro, OR, USA, in 2013. He was a Visiting Professor with the University of Michigan, Ann Arbor, MI, USA, from 2011 to 2012, the Berkeley Wireless Research Center, University of California at Berkeley, Berkeley, CA, USA, from 2009 to 2011, and the École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, in 2007. He is currently an Associate Professor with the National University of Singapore, Singapore, where he leads the Green IC Group and the Integrated Circuits and Embedded Systems area. He has authored or co-authored over 200 publications in journals and conference proceedings, and co-authored two books. His current research interests include ultra-low power VLSI circuits, self-powered and wireless nodes, near-threshold circuits for green computing, error-aware and widely energy-scalable VLSI circuits, and circuit techniques for emerging technologies.

Dr. Alioto was the Chair of the IEEE VLSI Systems and Applications Technical Committee, a Distinguished Lecturer, and a member of the Board of Governors of the Circuits and Systems Society. He served as a Guest Editor of various journal special issues, and has served as an Associate Editor of a number of IEEE and ACM journals. He is/was the Technical Program Chair of several conferences (e.g., ICECS, VARI, NEWCAS, and ICM) and the Track Chair (e.g., ICCD, ISCAS, ICECS, VLSI-SoC, APCCAS, and ICM).

Chirn Chye Boon (M'09–SM'10) received the B.E. (Hons.) and Ph.D. degrees in electrical engineering from Nanyang Technological University (NTU), Singapore, in 2000 and 2004, respectively.

He was a Senior Engineer with Advanced RFIC, Singapore. He has been at NTU since 2005, where he is currently an Associate Professor. He specializes in the areas of RF and millimeter-wave (MM-wave) circuits and systems design for biomedical and communications applications. He has conceptualized, designed and silicon-verified 74 circuits/chips for biomedical and communication applications. He has authored over 90 refereed publications in RF and MM-wave. He has co-authored a book *Design of CMOS RF Integrated Circuits and Systems* (World Scientific Publishing).

Dr. Boon serves as a committee member for various conferences. He is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He is on the Editorial Board of the *Journal of RF and Microwave Computer-Aided Engineering*. He is the Golden Reviewer of the IEEE Electron Devices Letters. He is the Programme Director of the RF and MM-wave research in the S$50million research centre of excellence, VIRTUS, NTU, since 2010. He is the Principal Investigator of the research grants of S$4,833,880.22. He is also one of the key NTU-team members of the MIT-NTU Joint Collaboration Project entitled Low Energy Electronic Systems, which has won the Singapore-MIT Alliance for Research and Technology International Research Grant proposal with a grant total of S$25million. He was the recipient of the Year-2 Teaching Excellence Award and Commendation Award for Excellent Teaching Performance from the School of Electrical and Electronic Engineering, NTU.

Chip-Hong Chang (S'92–M'98–SM'03) received the B.Eng. (Hons.) degree from the National University of Singapore, Singapore, in 1989, and the M.Eng. and Ph.D. degrees from Nanyang Technological University (NTU), Singapore, in 1993 and 1998, respectively.

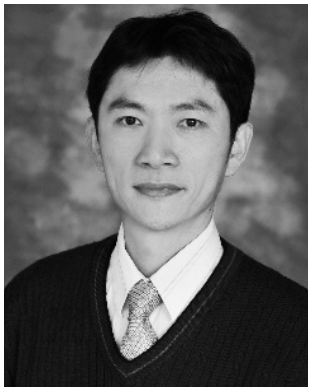
He served as a Technical Consultant in industry, prior to joining the School of Electrical and Electronic Engineering, NTU, in 1999, where he is currently an Associate Professor. He holds joint appointments with the university as an Assistant Chair of Alumni with the School of Electrical and Electronic Engineering from 2008 to 2014, the Deputy Director of the Center for High Performance Embedded Systems from 2000 to 2011, and the Program Director of the Center for Integrated Circuits and Systems from 2003 to 2009. His current research interests include hardware-oriented security, low-power arithmetic circuits, residue number system, and digital filter design.

Dr. Chang received the Collaboration Development Award for Microelectronics and Embedded Systems in April 2007 from the British High Commission of Singapore, the Research Collaboration Award by The Microsystems Strategic Alliance of Quebec and the Research Outcome Award Recognition twice from the Research Office of NTU. He is a fellow of the Institution of Engineering and Technology. He has served as an Associate Editor of the IEEE ACCESS, since 2013, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS since 2011, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS from 2010 to 2012, *Integration*, the *VLSI* journal from 2013 to 2015, and *Microelectronics* journal since 2014, an Editorial Advisory Board Member of the Open EEE Journal from 2007 to 2013, and an Editorial Board Member of the *Journal of Electrical Engineering Education* from 2008 to 2014. He also served as a Guest Editor for the special issue of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS in 2011, the *Journal of Circuits, Systems, and Computers* in 2011 and 2012, and over 40 international conference advisory and technical program committees. He was the co-recipient of two paper awards at PrimeAsia 2010 and the finalist of the Best Paper Award at VLSI'95. He has co-edited two books, published eight book chapters, and over 200 research papers (mostly in IEEE) in refereed international journals and conferences.

Naehyuck Chang (F'12) received the B.S., M.S., and Ph.D. degrees from the Department of Control and Instrumentation, Seoul National University, Seoul, Korea, in 1989, 1992, and 1996, respectively. He was with the Department of Computer Science and Engineering, Seoul National University, from 1997 to 2014, where he served as a Vice Dean of College of Engineering from 2011 to 2013. He is currently a Full Professor with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2014. His current research interests include low-power embedded systems and Design Automation of Things such as systematic design and optimization of energy storage systems and electric vehicles.

Dr. Chang is the Chair of the Association for Computing Machinery (ACM) Special Interest Group on Design Automation and an ACM Distinguished Scientist. He is the Editor-in-Chief of the *ACM Transactions on Design Automation of Electronics Systems*, and an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS. He also served as an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, the IEEE EMBEDDED SYSTEMS LETTERS, and the *ACM Transactions on Embedded Computing Systems*. He is (was) the General Co-Chair of VLSI-SoC, International Conference on Computer Design (ICCD) in 2014 and 2015, and the International Symposium on Low Power Electronics and Design in 2011. He is (was) Technical Program (Co-) Chair of the Asia and South Pacific Design Automation Conference in 2015, ICCD 2014, Hardware Software Codesign and System Synthesis in 2012, and International Symposium on Low-Power Electronics and Design (ISLPED) 2009.

Dr. Chang was a recipient of several ISLPED Low-Power Design Contest Awards, 2012 SAE Vincent Bendix Automotive Electronics Engineering Award, 2014 ISLPED Best Paper Award, and 2009 IEEE SSCS Seoul Chapter Award. He was a Research Professor with the LG Yonam Foundation in 2005.



Shih-Chieh Chang received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1987, and the Ph.D. degree in electrical and computer engineering from the University of California at Santa Barbara, Santa Barbara, CA, USA, in 1994.

He was elected as the President of the Taiwan Integrated Circuit Design Society from 2013 to 2014. He is currently a Full Professor and the Chairman of the Department of Computer Science with National Tsing Hua University, Hsinchu, Taiwan. He is also the Executive Director of the National Program for Intelligent Electronics and will be the Discipline Co-Ordinator of Microelectronic Area with the Ministry of Science and Technology, Taiwan, from 2015. He has authored more than 150 technical papers. His current research interests include design automation for low power, variation aware optimization and tolerance, and 3-D IC design methodology.

Dr. Chang is also an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS and was an Associate Editor of the *ACM Transactions on Design Automation of Electronic Systems*. He was the General Chair of the VLSI Design/CAD Symposium in 2006.

Yao-Wen Chang (S'94–A'96–M'96–SM'12–F'13) received the B.S. degree from National Taiwan University (NTU), Taipei, Taiwan, in 1988, and the M.S. and Ph.D. degrees from the University of Texas at Austin, Austin, TX, USA, in 1993 and 1996, respectively, all in computer science.

He was a Visiting Scholar with the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2014, and a Visiting Professor with Waseda University, Kitakyushu, Japan, from 2004 to 2011. He is currently an Associate Dean of the College of Electrical Engineering and Computer Science and a Distinguished Professor with the Department of Electrical Engineering, NTU. He was the Chairman of the Graduate Institute of Electronics Engineering, NTU, from 2010 to 2013. He co-edited one textbook on Electronic Design Automation, co-authored one book on routing, and over 250 ACM/IEEE conference/journal papers in these areas, including highly cited works on floorplanning, placement, routing, design for manufacturability, and field-programmable gate array. His NTUplace3 placer was the core engine of the popular Digital Custom Placer of SpringSoft, acquired by the #1 EDA vendor, Synopsys, in 2012, for over $400 million U.S. His current research interests include VLSI physical design and design for manufacturability/reliability.

Dr. Chang was a recipient of four awards at the 50th ACM/IEEE Design Automation Conference (DAC) in 2013, including the 1st Most Papers in the 5th Decade (34 DAC papers in the 5th decade; #1 worldwide). He was the 1st-place winner of five recent major EDA Contests: the 2013 IEEE CAD Contest at the International Conference on Computer-Aided Design (ICCAD) (Legalization and Detailed Placement), the 2012 ACM/IEEE DAC Routability-Driven Placement Contest, the 2012 ACM International Symposium on Physical Design (ISPD) Discrete Gate Sizing Contest, the 2011 IEEE CEDA PATMOS Timing Analysis Contest, and the 2009 ACM ISPD Clock Network Synthesis Contest. He has received 15 other top-3 contest awards during the past eight years. He was a recipient of six Best Paper Awards and the 2007 IEEE/ACM ICCAD Professor Margarida Jacome Memorial Award. He has received 22 Best Paper Award Nominations from top international conferences, including DAC (five times), ICCAD (four times), and ISPD (five times) since 2000. He has received many research awards, such as the Distinguished Research Awards (highest honor) from the Ministry of Science and Technology of Taiwan (three times), and the IBM Faculty Awards (three times), the 2009 Distinguished EE Professor from the CIEE, the 2004 MXIC Young Chair Professorship from the MXIC Corporation, and Distinguished Teaching Award (highest honor for top 1% teachers)/Excellent Teaching Awards (eight times). He was an Editor of the IEEE DESIGN AND TEST OF COMPUTERS from 2012 to 2014 and was an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS from 2008 to 2013. He has served as the Steering Committee/General/Program Chair of ISPD, and the General/Program Chair of ICCAD, and the Program Chair of ASP-DAC and FPT. He is on the IEEE Council of EDA (CEDA) and ICCAD Executive Committees, the ASP-DAC Steering Committee, and has served on the Technical Program Committees of all major EDA conferences. He is currently the IEEE CEDA Vice President of Technical Activities. He has served as the Chair of the EDA Consortium of the Ministry of Education of Taiwan and an Independent Board Director of Genesys Logic, Inc., New Taipei City, Taiwan, a Technical Consultant of MediaTek Inc., Hsinchu, Taiwan, RealTek Semiconductor Corporation, Hsinchu, and Faraday Technology Inc., Hsinchu, Taiwan.

Poki Chen (M'05) was born in Chiayi, Taiwan, in 1963. He received the B.S., M.S., and Ph.D. degrees from the Department of Electrical Engineering, National Taiwan University (NTU), Taipei, Taiwan, in 1985, 1987 and 2001, respectively.

He was a Lecturer, an Assistant Professor, and an Associate Professor with the Department of Electronic Engineering, National Taiwan University of Science and Technology (NTUST), Taipei, from 1998 to 2011, where he is currently a Professor with the Department of Electronic and Computer Engineering. He was the Director of the System-on-Chip Research Center/Business Incubation Center, NTUST, since 2010. He is interested in creating innovative analog applications for field-programmable gate array (FPGA) platforms, such as FPGA smart temperature sensor, FPGA digital-to-time, and time-to-digital converters. His current research interests include analog/mixed-signal integrated circuits and systems with a special interest focused on time-domain signal processing circuits, such as time-domain smart temperature sensor, time-to-digital converter, digital pulse generator, digital pulse width modulator, and duty cycle corrector.

Dr. Chen serves as the Chair of the Department of Electronic and Computer Engineering, NTUST, and an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS and the IEEE ACCESS. He also serves on the Editorial Board of the *International Scholarly Research Network Electronics*. He is the Organizer of the IEEE International Conference on Intelligent Green Building and Smart Grid, and serves as the TPC Member and the Session Chair of various IEEE conferences, such as the International System-on-Chip Conference, the International Symposium on VLSI Design, Automation and Test, the International Future Energy Electronics Conference, Nordic Mediterranean Workshop on Time to Digital Converters, the International Symposium on Next-Generation Electronics, and the International Conference on Anti-Counterfeiting, Security and Identification.

Masud H. Chowdhury (S'00–M'04–SM'09) received the B.S. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology, Bangladesh, Dhaka, in 1998, and the Ph.D. degree in computer engineering from Northwestern University, Evanston, IL, USA, in 2004.

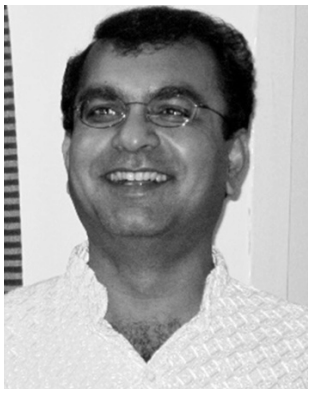
He is currently an Associate Professor with the Department of Computer Science and Electrical Engineering, University of Missouri–Kansas City, Kansas City, MO, USA. He has authored over 100 articles in various journals and conferences in his field of research, which includes high performance issues of deep submicron and nanoscale integrated circuits, emerging interconnect and device technologies, on-chip voltage regulation, ultralow-power circuit design, multicore design issues, and the next-generation post-silicon circuits and devices-based ferroelectric materials, and 2-D super-material like graphene and molybdenum disulfide.

Dr. Chowdhury serves as the Chair of the IEEE VLSI Systems and Applications Technical Committee. He also serves as an Associate Editors of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION, the *Microelectronics* (Elsevier) journal, and the *Journal of Circuits, Systems, and Signal Processing* (Springer). He was the Symposium Chair of the Computer Design and VLSI Symposium in the 2009 World Congress on Computer Science and Information Engineering. He has organized several special sessions and chaired over 40 sessions in a number of conferences. He is currently the TPC member of the IEEE VLSI track and five other conferences.

Pasquale Corsonello received the master's degree in electronics engineering from the University of Naples Federico II, Naples, Italy, in 1988.

He joined the Institute of Research on Parallel Computers, National Council of Research of Italy, Naples, where he was working on the design and modelling of electronic transducers for high precision measurement, receiving a postgraduate two-years grant. In 1992, he joined the Department of Electronics, Computer Science and Systems, University of Calabria, Rende, Italy, as a Research Associate. In 1997, he was appointed as an Assistant Professor of Electronics with the Department of Electronics Engineering and Applied Mathematics, University of Reggio Calabria, Reggio Calabria, Italy, where he also served as the Director of the Microelectronics Laboratory. In 2001, he was appointed as an Associate Professor of Electronics and the Chair of the Ph.D. Program in Electronics Engineering with the University of Reggio Calabria. In 2004, he was a Visiting Researcher with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY, USA. In 2005, he was appointed as an Adjunct Associate Professor with the Department of Electrical and Computer Engineering. He is currently an Associate Professor of Electronics with the Department of Informatics, Modeling, Electronics and System Engineering, University of Calabria. He has co-authored over 140 technical papers, and holds two patents in these fields. One of these papers is among the 25 most downloaded TVLSI papers in 2007. His current research interests include high-performance low-power CMOS design, VLSI architecture for image and video processing, and emerging nanoarchitectures.

Prof. Corsonello was a co-recipient of five best paper awards. He has also received several grants from both private industries and government agencies for projects in these areas. He serves on the Technical Committees of several VLSI conferences, and as a peer reviewer for several VLSI journals. He is also an Associate Editor of the *Journal of Low Power Electronics and Applications*.



Vivek De (F'11) received the B.Tech. degree from IIT Madras, Chennai, India, in 1985, the M.S. degree from Duke University, Durham, NC, USA, in 1986, and the Ph.D. degree from the Rensselaer Polytechnic Institute, Troy, NY, USA, in 1991, all in electrical engineering.

He is currently an Intel Fellow and the Director of Circuit Technology Research with Intel Labs, Hillsboro, OR, USA. He is responsible for providing strategic technical directions for long-term research in future circuit technologies and leading energy efficiency research across the hardware stack. He has authored 227 publications in refereed international conferences and journals, and holds 197 patents, with 29 more patents filed (pending).

Dr. De received the Intel Achievement Award for his contributions to an integrated voltage regulator technology. He was a recipient of the Best Paper Award at the 1996 IEEE International ASIC Conference, and nominated for Best Paper Awards at the 2007 IEEE/ACM Design Automation Conference (DAC), and the 2008 IEEE/ACM International Conference on Computer-Aided Design. One of his publications was recognized in the 2013 IEEE/ACM Design Automation Conference as one of the Top 10 Cited Papers in 50 Years of DAC. He served as the General Chair/Co-Chair in 2013 and 2014, the Program Chair/Co-Chair in 2011 and 2012 of the Symposium on VLSI Circuits, and a Executive Committee Member of the VLSI Symposia from 2011 to 2015. He has been a member of the ISSCC High Performance Digital Subcommittee since 2013. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 2008 to 2010, and has been an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS since 2014.

Masahiro Fujita received the Ph.D. degree in information engineering from the University of Tokyo, Tokyo, Japan, in 1985, with a focus on model checking of hardware designs using logic programming languages.

He joined Fujitsu, Tokyo, as a Researcher, in 1985, where he started to work on hardware automatic synthesis and formal verification methods and tools, including enhancements of BDD/SAT-based techniques. From 1993 to 2000, he was the Director with the Fujitsu Laboratories of America, Inc., Sunnyvale, CA, USA, and headed the Hardware Formal Verification Group, where he developed a formal verifier for real-life designs having more than several million gates. The developed tool has been used in production internally at Fujitsu and externally as well. Since 2000, he has been a Professor with the VLSI Design and Education Center, University of Tokyo. He has done innovative work in the areas of hardware verification, synthesis, testing, and software verification-mostly targeting embedded software and Web-based programs. He has been involved in the Japanese governmental research project for dependable system designs and has developed a formal verifier for C programs that could be used for both hardware and embedded software designs. The tool is under evaluation jointly with industry under governmental support. He has authored or co-authored 10 books, and over 200 publications. His current research interests include synthesis and verification in system-on-a-chip, hardware/software co-designs targeting embedded systems, digital/analog co-designs, and formal analysis, verification, and synthesis of Web-based programs, and embedded programs.

Dr. Fujita has been involved as the Program and Steering Committee Member in many prestigious conferences on CAD, VLSI designs, and software engineering.

Ranjit Gharpurey (M'95–SM'10) received the B.Tech. degree from IIT Kharagpur, Kharagpur, India, in 1990, and the M.S. and Ph.D. degrees from the University of California at Berkeley, Berkeley, CA, USA, in 1992 and 1995, respectively.

He was with Texas Instruments Incorporated, Dallas, TX, USA, from 1995 to 2003. He was an Assistant Professor with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI, USA, from 2003 to 2005. He is currently a Professor with the Department of Electrical and Computer Engineering, University of Texas at Austin, Austin, TX, USA. His current research interests include analog circuit design, with an emphasis on RF and wireless communication applications, low-power design techniques, and techniques for improving efficiency, and dynamic range in analog circuits. He has numerous publications and patents in these areas.

Prof. Gharpurey was a co-recipient of the Best Student Paper Awards at the RFIC Symposium in 2008 (first place) and the IEEE Sensors Conference in 2005 (second place). He was also a co-recipient of the Best Paper Award from the IEEE JOURNAL OF SOLID-STATE CIRCUITS for 2008. He served as an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, and a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He has served on the Program Committees of the Custom Integrated Circuits Conference and the International Solid-State Circuits Conference, and is currently on the Program Committee of the IEEE Radio Frequency Integrated Circuits Symposium.

Said Hamdioui (M'99–SM'11) received the M.S.E.E. and Ph.D. degrees (Hons.) from the Delft University of Technology (TUDelft), Delft, The Netherlands, in 1997 and 2001, respectively.

He is currently co-leading dependable-nano computing research activities with the Computer Engineering Laboratory, TUDelft. Prior to joining TUDelft, he spent many years in industry; he was with Intel Corporation, Santa Clara, CA, USA, Philips Semiconductors R&D, Crolles, France, and Philips/NXP Semiconductors, Nijmegen, The Netherlands. He has authored one book and co-authored over 130 conference and journal papers. He has consulted for many semiconductor companies, such as Intel, San Jose, CA, USA, STMicroelectronics, Crolles, France, Altera, San Jose, CA, USA, Atmel, Rousset, France, Renesas, Tokyo, Japan, etc. He is strongly involved in the international test technology community; he delivered dozens of keynote speeches, distinguished lectures, and invited presentations and tutorials at major international forums/conferences and leading semiconductor companies. His current research interests include nanocomputing, VLSI test, reliability, hardware security, and memristor technology.

Dr. Hamdioui serves on the editorial board of the *Journal of Electronic Testing: Theory and Applications*, and on that of IEEE DESIGN & TEST. He is also a member of Association for European NanoElectronics Activities/ European Nanoelectronics Initiative Advisory Council Scientific Committee Council.

Masanori Hashimoto (S'00–A'01–M'03–SM'11) received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively.

He has been an Associate Professor with the Department of Information Systems Engineering, Osaka University, Osaka, Japan, since 2004. His current research interests include computer-aided design for digital integrated circuits, design for manufacturability and reliability, timing and power integrity analysis, and low-power circuit design.

Dr. Hashimoto is a member of the Association for Computing Machinery, the Institute of Electronics, Information, and Communication Engineers, and the Information Processing Society of Japan (IPSJ). He was a recipient of the Best Paper Award at the Asia and South Pacific-Design Automation Conference (ASP-DAC) in 2004. He was on the Technical Program Committees of international conferences, including the DAC, International Conference on Computer-Aided Design, ASP-DAC, Design Automation and test in Europe, International Symposium on Physical Design, International Test Conference, and Symposium on VLSI Circuits. He currently serves as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, and the *IEICE Transactions on Fundamentals*, and an Associate Editor-in-Chief of the *IPSJ Transactions on System LSI Design Methodology*.

Tsung-Yi Ho (M'08–SM'12) received the Ph.D. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2005.

He was with National Cheng Kung University, Tainan, Taiwan, from 2007 to 2014. He is currently a Professor with the Department of Computer Science, National Chiao Tung University, Hsinchu, Taiwan. His current research interests include design automation for microfluidic biochips and nanometer integrated circuits.

Dr. Ho has received many research awards, such as the Dr. Wu Ta-You Memorial Award of National Science Council of Taiwan, the Junior Research Investigators Award of the Academia Sinica, the Distinguished Young Scholar Award of the Taiwan IC Design Society, the Outstanding Young Electrical Engineer Award of the Chinese Institute of Electrical Engineering, the Delta Electronics K. T. Li Research Award, the ACM Taipei Chapter Young Researcher Award, the IEEE Tainan Chapter Gold Member Award, the Invitational Fellowship of the Japan Society for the Promotion of Science, the Humboldt Research Fellowship by the Alexander von Humboldt Foundation, and the Hans Fischer Fellow by the Institute of Advanced Study of the Technical University of Munich. He has presented eight tutorials and contributed five special sessions in ACM/IEEE Conferences, all in design automation for microfluidic biochips. He currently serves as an ACM Distinguished Speaker, a Distinguished Visitor of the IEEE Computer Society, the Chair of the IEEE Computer Society Tainan Chapter, the Chair of the ACM Special Interest Group on Design Automation Taiwan Chapter, and an Associate Editor of the *ACM Journal on Emerging Technologies in Computing Systems*, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, a Guest Editor of the IEEE DESIGN AND TEST OF COMPUTERS, and the Technical Program Committees of major conferences, including Design Automation Conference (DAC), International Conference on Computer-Aided Design (ICCAD), Asia and South Pacific-DAC (ASP-DAC), Design Automation and Test in Europe (DATE), International Symposium on Physical Design (ISPD), and International Conference on Computer Design (ICCD), VLSI Design, VLSI-DAT, VLSI-SoC, and SOCC.

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Dr. Hwang has served on the Editorial Board of *Active and Passive Electronic Components* since 2010, the Editorial Board of the *Journal of Engineering* since 2012, and the Editorial Board of the *Far East Journal of Electronics and Communications and the International Scholarly Research Notices* since 2013. He has served as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, and the IEEE ACCESS online open access mega-journal since 2013. He has served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–II since 2014. He was a Technical Program Committee Member of VLSI Design/CAD Symposium in Taiwan from 2010 to 2014.

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He has successfully led pervasive statistical methodology for yield prediction and also the technology-driven SRAM at IBM Server Group. He commercialized these techniques. He is currently a Research Staff Member with the Thomas J. Watson Research Center, IBM, Yorktown Heights, NY, USA. His novel interconnects processes and structures for aluminum, tungsten and copper technologies, which are widely used in IBM for various technologies from sub-0.5 μm to 14 nm. He has authored or co-authored over 175 papers. He holds 54 invention plateaus, and has over 200 U.S. patents, and over 350 including international patents.

Dr. Joshi is a fellow of the International Symposium on Quality Electronic Design and distinguished alumnus of IIT Bombay. He received three Outstanding Technical Achievement and three Highest Corporate Patent Portfolio Awards for licensing contributions. He was inducted into the New Jersey Inventor Hall of Fame in 2014 along with pioneer Nicola Tesla. He was a recipient of the 2013 IEEE CAS Industrial Pioneer Award and the 2013 Mehboob Khan Award from Semiconductor Research Corporation. He is a member of the IBM Academy of Technology and a Master Inventor. He is a Distinguished Lecturer of the IEEE CAS and EDS Society. He serves as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS. He served on committees of the International Symposium Low Power Electronic Design, the IEEE VLSI Design, the IEEE Custom Integrated Circuits Conference, the IEEE International SOI Conference, International Symposium on Quality Electronic Design, and Advanced Metallization Program committees. He served as the General Chair of the IEEE International Symposium on Low-Power Electronics and Design. He is an industry liaison for universities as a part of the Semiconductor Research Corporation. He is also in the industry liaison committee of the IEEE Circuits and Systems Society.

Tanay Karnik (M'88–SM'04–F'13) received the Ph.D. degree in computer engineering from the University of Illinois at Urbana-Champaign, Champaign, IL, USA.

He joined Intel Corporation, Hillsboro, OR, USA, in 1995. He is currently the Director of the University Research Office and a Principal Engineer with Intel Labs. He has authored over 80 technical papers, and holds 55 issued and 28 pending patents. His current research interests include variation tolerance, power delivery, soft errors, and physical design.

Dr. Karnik is an International Symposium on Quality Electronic Design (ISQED) Fellow, and an Associate Editor of the IEEE TRANSACTION ON VERY LARGE SCALE INTEGRATION, and was a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He received the Intel Achievement Award for the pioneering work on integrated power delivery. He has presented several keynotes, invited talks, and tutorials, and has served on six Ph.D. students' committees. He was a member of the International Solid-State Circuits Conference, the Design Automation Conference, the International Conference on Computer-Aided Design, the International Conference on IC Design and Technology, and ISQED Program Committees, and the IEEE JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, the IEEE TRANSACTION ON VERY LARGE SCALE INTEGRATION, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I review committees. He was the General Chair of the International Symposium on Low Power Electronics and Design in 2014, the Asia Symposium on Quality Electronic Design in 2010, ISQED in 2008 and 2009, and the International Conference on IC Design and Technology in 2008.

Chulwoo Kim received the B.S. and M.S. degrees in electronics engineering from Korea University, Seoul, Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Champaign, IL, USA, in 2001.

He was an Intern with the Design Technology, Intel Corporation, Santa Clara, CA, USA, in 1999. In 2001, he joined IBM Microelectronics Division, Austin, TX, USA, where he was involved in cell processor design. Since 2002, he has been with the Department of Electronics and Computer Engineering, Korea University, where he is currently a Professor. He was a Visiting Professor with the University of California at Los Angeles, Los Angeles, CA, USA, in 2008, and the University of California at Santa Cruz, Santa Cruz, CA, USA, in 2012. His current research interests include wireline transceiver, memory, power management, and data converters.

Dr. Kim was a recipient of the Samsung HumanTech Thesis Contest Bronze Award in 1996, the ISLPED Low-Power Design Contest Award in 2001, the DAC Student Design Contest Award in 2002, the SRC Inventor Recognition Awards in 2002, the Young Scientist Award from the Ministry of Science and Technology of Korea in 2003, the Seoktop Award for excellence in teaching in 2006 and 2011, and the ASP-DAC Best Design Award in 2008. He is currently on the Editorial Board of the IEEE TRANSACTIONS ON VLSI SYSTEMS and the Technical Program Committee of the IEEE International Solid-State Circuits Conference.

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He was with Cypress Semiconductors, Bangalore, India, from 2004 to 2005, where he was involved in micro-power SRAM designs. He is currently a Staff Research Scientist with the Circuit Research Laboratory, Intel Corporation, Hillsboro, OR, USA. His current research interests include low-power/low-voltage logic, memory circuits, and power management circuits.

Dr. Kulkarni was the recipient of the 2004 Best M.Tech. Student Award from IISc Bangalore, the 2008 Semiconductor Research Corporation (SRC) Inventor Recognition Award, the 2008 International Symposium on Low Power Electronics and Design (ISLPED) Design Contest Award, the 2008 Intel Foundation Ph.D. Fellowship Award, the Best Paper in Session Award from the 2008 SRC TECHCON, the 2010 Outstanding Doctoral Dissertation Award from the School of Electrical and Computer Engineering, Purdue University, the 2012 Intel Patent Recognition Award, and four Intel Divisional Recognition Awards. He is also a Technical Program Committee Member of the ISLPED and Asian Solid-State Circuits Conference and serves as an industrial liaison at the SRC, integrated circuits and systems track.

Erik Larsson received the M.Sc., Licentiate of Engineering, and Ph.D. degrees from Linköping University, Linköping, Sweden, in 1994, 1998, and 2000, respectively.

He was with Linköping University as an Assistant Professor from 2003 to 2005, and as an Associate Professor from 2006 to 2011. He received a scholarship from the Swedish Foundation for Strategic Research for a sabbatical at NXP Semiconductors, The Netherlands, from 2008 to 2010. He is currently an Associate Professor (Docent) with the Department of Electrical and Information Technology, Lund University, Lund, Sweden.

Dr. Larsson received the Institution of Engineering and Technology Premium Award in 2009, and the Best Paper Award at the IEEE Asian Test Symposium (ATS) in 2002. He authored a book entitled *Introduction to Advanced System-on-Chip Test Design and Optimization* (Springer, 2005), and supervised the thesis that received the Best Master thesis in Engineering in Sweden (Lilla Polhemspriset, 2008). He received a scholarship from the Japan Society for the Promotion of Science for a Post-Doctoral Researcher at the Nara Institute of Science and Technology, Japan, from 2001 to 2002. He has served on major conferences, like the International Test Conference (ITC), Design Automation and Test in Europe (DATE), VLSI Design, VLSI Test Symposium (VTS), European Test Symposium (ETS), ATS, VLSI-SoC, Great Lake Symposium on VLSI (GLSVLSI), and the Design and Diagnostics of Electronic Circuits and Systems. He was the Program Chair of ETS in 2011, the Vice Program Chair of ETS in 2010, and the Topic Chair at DATE, ETS, VLSI Design, and GLSVLSI. He has served as a Guest Editor of the special issue on Emerging Strategies for Resource-Constrained Testing of System Chips in the IEE Proceedings for Computer and Digital Techniques.

Hai (Helen) Li received the B.S. and M.S. degrees in microelectronics from Tsinghua University, Beijing, China, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA, in 2004.

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Dr. Li received the four Best Paper Awards and five Best Paper Nominations from ISQED, ISLPED, DATE, ISVLSI, ASPDAC, and ICCAD. She is an Associate Editor of the *ACM Transactions on Design Automation of Electronic Systems* and has served as technical program committee members for more than 20 international conference series. She was the recipient of NSF CAREER Award in 2012 and DARPA YFA Award in 2013.

Huawei Li (M'00–SM'09) received the B.S. degree in computer science from Xiangtan University, Hunan, China, in 1996, and the M.S. and Ph.D. degrees from the Institute of Computing Technology (ICT), Chinese Academy of Sciences (CAS), Beijing, China, in 1999 and 2001, respectively.

She visited the University of California at Santa Barbara, Santa Barbara, CA, USA, from 2009 to 2010. She has been a Professor with ICT, CAS, since 2008. She has published over 120 technical papers, and holds 20 Chinese Patents. Her current research interests include testing of VLSI/system-on-a-chip circuits, design verification, design for reliability, and error tolerant computing.

Dr. Li currently serves on the Editorial Board of the *Journal of Computer-Aided Design and Computer Graphics* (in Chinese), and the *Journal of Computer Research and Development* (in Chinese). She was the Technical Program Co-Chair of the IEEE Asian Test Symposium in 2007 and the General Co-Chair in 2014. She was the Technical Program Chair of the IEEE Workshop on RTL and High Level Testing (WRTLT) in 2003 and the Technical Program Vice Chair in 2013. She has served as the Steering Committee Chair of WRTLT since 2014, as the Secretary General of the China Computer Federation Technical Committee on Fault-Tolerant Computing since 2008, and on the technical program committees for several IEEE conferences.

Mohammad M. Mansour (S'97–M'03–SM'08) received the B.E. (Hons.) and the M.E. degrees in computer and communications engineering from the American University of Beirut (AUB), Beirut, Lebanon, in 1996 and 1998, respectively, and the M.S. degree in mathematics and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana—Champaign (UIUC), Champaign, IL, USA, in 2002 and 2003, repsectively.

He was a Visiting Researcher at Broadcom in 2012. He was on research leave with Qualcomm Flarion Technologies, Bridgewater, NJ, USA, from 2006 to 2008, where he was involved in modem design and implementation for 3GPP-LTE, 3GPP-UMB, and peer-to-peer wireless networking PHY layer standards. He was a Research Assistant at the Coordinated Science Laboratory, UIUC, from 1998 to 2003. He was with National Semiconductor Corporation, San Francisco, CA, USA, with the Wireless Research Group in 2000. He was a Research Assistant with the Department of Electrical and Computer Engineering, AUB, in 1997. He joined as a faculty member with AUB in 2003. He was a Teaching Assistant at the Department of Electrical and Computer Engineering. He is currently an Associate Professor with the Department of Electrical and Computer Engineering, AUB. He was on research leave in industry at Broadcom Corporation, Sunnyvale, CA, USA, in 2013, where he was involved in 4G LTE modem design. His current research interests are VLSI design and implementation for embedded signal processing and wireless communications systems, coding theory and its applications, digital signal processing systems, and general purpose computing systems.

Prof. Mansour is a member of the Design and Implementation of Signal Processing Systems Technical Committee Advisory Board of the IEEE Signal Processing Society. He served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2008 to 2013. He currently serves as an Associate Editor of the IEEE TRANSACTIONS ON VLSI SYSTEMS since 2011, and an Associate Editor of the IEEE SIGNAL PROCESSING LETTERS since 2012. He served as the Technical Co-Chair of the IEEE Workshop on Signal Processing Systems in 2011, and as a member of the Technical Program Committee of various international conferences. He was the recipient of the PHI Kappa PHI Honor Society Award twice in 2000 and 2001, and the recipient of the Hewlett Foundation Fellowship Award in 2006.

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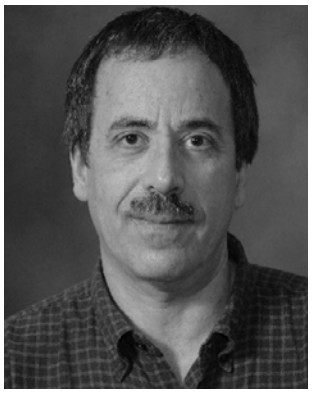
He is an Associate Professor with the Department of Computer and Information Science and Engineering, University of Florida, Gainesville, FL, USA. He has authored four books, ten book chapters, and over 100 research articles in premier international journals and conferences. His current research interests include design automation of embedded systems, energy-aware computing, hardware–software verification, security and reliability, and post-silicon debug.

Prof. Mishra was a recipient of several awards, including the National Science Foundation CAREER Award, two Best Paper Awards (International Conference on Co-design and System Synthesis 2003 and International Conference on VLSI Design 2011), and 2004 EDAA Outstanding Dissertation Award from the European Design Automation Association. He has also received the 2007 International Educator of the Year Award from the UF College of Engineering for his significant international research and teaching contributions. He currently serves as the Deputy Editor-in-Chief of *IET Computers and Digital Techniques*. He is an Associate Editor of *ACM Transactions on Design Automation of Electronic Systems*, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, the IEEE DESIGN AND TEST, and the JOURNAL OF ELECTRONIC TESTING. He is a Technical Program Committee Member of several international conferences, including Design Automation Conference, International Conference on Computer-Aided Design, Design Automation and test in Europe, International Symposium on Hardware/Software Codesign and System Synthesis, and VLSI Design. He has also served as the General Chair of the IEEE High Level Design Validation and Test (HLDVT) 2010, the Program Chair of HLDVT 2009, and a Guest Editor of the IEEE TRANSACTIONS ON COMPUTERS, the IEEE DESIGN AND TEST, the *Journal of Electronic Testing*, and the *International Journal of Parallel Programming*. He is a Senior Member of ACM.



Steven M. Nowick (F'09) received the B.A. degree from Yale University, New Haven, CT, USA, and the Ph.D. degree in computer science from Stanford University, Stanford, CA, USA, in 1993.

He is currently a Professor of Computer Science and Electrical Engineering with Columbia University, New York, NY, USA, and the former chair and co-founder of the Computer Engineering Program. His current projects include scalable networks-on-a-chip for shared-memory parallel processors and embedded systems, ultra low-power energy digital systems, fault tolerance, and low-power and robust global communication. His current research interests include design methodologies and CAD tools for synthesis and optimization of asynchronous and mixed-timing (i.e., GALS) digital systems. He holds 12 issued U.S. patents.

Dr. Nowick is a Senior Member of the Association for Computing Machinery. He was a recipient of an Alfred P. Sloan Research Fellowship, and the NSF CAREER and RIA Awards. He was also a recipient of the Best Paper Awards at the IEEE International Conference on Computer Design in 1991 and 2012, and the IEEE Async Symposium in 2000. He co-founded the IEEE Async Symposia series in 1994, and was its Program Committee Co-Chair and General Co-Chair. He was also the Program Chair of the IEEE/ACM International Workshop on Logic and Synthesis and the Program Track/Subcommittee Chair at DAC, DATE and ICCD conferences. He is currently an Associate Editor of the IEEE DESIGN & TEST MAGAZINE, the *ACM Journal on Emerging Technologies in Computer Systems* and the IEEE TRANSACTIONS ON VLSI SYSTEMS, and was formerly an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN. He was Selection Committee Chair of the ACM/SIGDA Outstanding Dissertation in EDA Award, and a member of the Best Paper award committees of DAC and ICCAD conferences. He was a recipient of the Columbia Engineering School Alumni Distinguished Faculty Teaching Award.

Michael Orshansky (F'14) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer sciences from the University of California at Berkeley, Berkeley, CA, USA, in 1996, 1998, and 2001, respectively.

He was a Research Scientist and Lecturer with the Department of Electrical and Computer Science, UC Berkeley, in 2003. He is currently a Professor of Electrical and Computer Engineering with the University of Texas, Austin, TX, USA, and holds the John E. Kasch Endowed Faculty Fellowship in Engineering. He has published over 90 technical articles and holds three U.S. patents. He has authored a book entitled *Design for Manufacturability and Statistical Design: A Constructive Approach*. His current research interests include low-power design, hardware security, approximate computing, design optimization for robustness and manufacturability, and statistical analysis and design methods.

Dr. Orshansky was a recipient of a number of awards for his research contributions and professional services, including the National Science Foundation CAREER Award in 2004, the ACM Special Interest Group on Design Automation Outstanding New Faculty Award in 2007, the ACM Recognition of Service Award in 2007, the University of Texas Faculty Research Award in 2004, the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING Best Paper Award in 2004, the Best Paper Award at the Design Automation Conference in 2005, the Best Paper Award at the International Symposium on Quality Electronic Design in 2006, and the IEEE/ACM William J. McCalla Best Paper Award at the International Conference on Computer-Aided Design in 2006. He has served as an Associate Editor for the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, the Vice President for Technical Activities of the IEEE Council on Electronic Design Automation, the General Chair of ACM/IEEE International Workshop on Timing Issues in Digital Systems, and the Chair of Technical Program Subcommittees at the International Conference on Computer-Aided Design, Design Automation Conference, International Conference on IC Design and Technology, and International Conference on Computer Design.

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He is a Professor and holder of the Boeing Centennial Chair in Computer Engineering with the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA, USA. His current research interests include novel interconnect architectures for multicore chips, ON-chip wireless communication networks, and hardware accelerators for biocomputing.

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From 1992 to 1997, he was with the faculty of the Department of Electrical and Computer Engineering with Iowa State University, Ames, IA, USA. Since 1997, he has been with the University of Minnesota, where he currently holds the Distinguished McKnight University Professorship and the Robert and Marjorie Henle Chair in Electrical and Computer Engineering. He has authored or edited nine books and has published widely in the area of computer-aided design of VLSI circuits.

Dr. Sapatnekar has served as the General Chair and Technical Program Chair of the ACM/EDAC/IEEE Design Automation Conference, the ACM International Symposium on Physical Design, and the IEEE/ACM International Workshop on the Specification and Synthesis of Digital Systems, and as the Technical Program Chair of the International Conference on VLSI Design. He has served with the editorial boards of several publications, including the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN as the Editor-In-Chief, the IEEE DESIGN AND TEST, the IEEE TRANSACTIONS ON VLSI SYSTEMS, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II. His research has been recognized with the NSF CAREER Award, six conference Best Paper Awards and a Best Poster Award, and an International Conference on Computer-Aided Design 10-year Retrospective Most Influential Paper Award. He has received a Fulbright Award to Spain, the Semiconductor Research Corporation Technical Excellence Award, and the Semiconductor Industry Association University Researcher Award.

Ioannis Savidis received the B.S.E. degree in electrical and computer engineering and biomedical engineering from Duke University, Durham, NC, USA, in 2005, and the M.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Rochester, Rochester, NY, USA, in 2007 and 2013, respectively.

He was with the 3-D Integration Group, Freescale Semiconductor, Austin, TX, USA, in 2007, and the System on Package and 3-D Integration Group, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA, in 2008, 2009, 2010, and 2011. He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA, USA, where he directs the Integrated Circuits and Electronics Design Laboratory. His current research interests include analysis, modeling, and design methodologies for high performance digital and mixed-signal integrated circuits, power management for system-on-a-chip and microprocessor circuits (including on-chip dc-dc converters), emerging integrated circuit technologies, integrated circuits (IC) design for trust (hardware security), and interconnect related issues in 2-D and 3-D ICs.

Dr. Savidis is a member of the Editorial Boards of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, the *Microelectronics* journal, and the *Journal of Circuits, Systems and Computers*.

Aida Todri-Sanial (M'03) received the B.S. degree in electrical engineering from Bradley University, Peoria, IL, USA, in 2001, the M.S. degree in electrical engineering from Long Beach State University, Long Beach, CA, in 2003, and the Ph.D. degree in electrical and computer engineering from the University of California, Santa Barbara, CA, USA, in 2009.

She was a Research and Development Engineer with the Fermi National Accelerator Laboratory, Batavia, IL, USA. She has also held visiting research positions at Mentor Graphics, San Jose, CA, USA, Cadence Design Systems, San Jose, CA, USA, STMicroelectronics, Grenoble, France, and the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA. She is currently a Research Scientist for French National Council of Scientific Research (CNRS) attached to Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier. Her current research interests include nanometer-scale issues in high performance VLSI design with an emphasis on power, thermal, signal integrity and reliability issues, and on circuits and systems for emerging technologies.

Dr. Todri-Sanial was a recipient of the John Bardeen Fellowship in Engineering in 2009 and CNRS Prime d'Excellence Scientifique in 2012. She serves as a Technical Program Committee Member of the Computer Society Annual Symposium on VLSI, NEWCAS, Great Lakes Symposium on VLSI, the International Symposium on Quality Electronic Design, the International Conference on Electron Devices and Solid-State Circuits, and Design Automation and test in Europe.

Xiaoqing Wen (M'89–SM'08–F'12) received the B.E. degree from Tsinghua University, Beijing, China, in 1986, the M.E. degree from Hiroshima University, Hiroshima, Japan, in 1990, and the Ph.D. degree from Osaka University, Suita, Japan, in 1993.

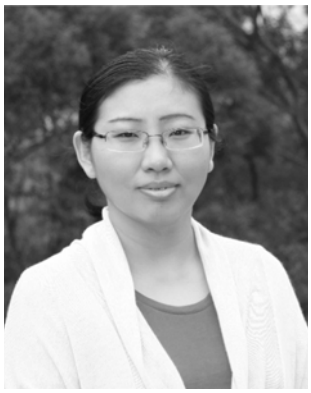
He was an Assistant Professor with Akita University, Akita, Japan, from 1993 to 1997. He was also a Visiting Researcher with the University of Wisconsin, Madison, WI, USA, from 1995 to 1996. He joined SynTest Technologies, Inc., Sunnyvale, CA, USA, in 1998, and served as its Chief Technology Officer until 2003. He joined Kyushu Institute of Technology, Iizuka, Japan, in 2004, where he is currently a Professor and the Director of the Dependable Integrated Systems Research Center. His current research interests include VLSI testing, diagnosis, and testable designs. He holds 38 U.S. patents and 14 Japan patents on VLSI testing.

Dr. Wen received the IEICE-ISS Best Paper Award in 2008. He is the Co-Chair of the Technical Activity Committee on Power-Aware Testing under the Test Technology Technical Council of the IEEE Computer Society. He has been an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS since 2012.

Jiang Xu (S'02–M'07) received the Ph.D. degree from Princeton University, Princeton, NJ, USA. He was with Bell Labs, Murray Hill, NJ, USA, from 2001 to 2002, as a Research Associate and discovered the First Generation Dilemma in platform-based system-on-chip (SoC) design methodologies.

He was a Research Associate with NEC Laboratories America, Princeton, NJ, USA, from 2003 to 2005, where he was involved in network-on-chip (NoC) designs and implementations. He joined a startup company, Sandbridge Technologies, Tarrytown, NY, USA, from 2005 to 2007, and worked on the development and implementation of two generations of NoC-based ultralow-power Multiprocessor SoC for mobile platforms. He established Mobile Computing System Laboratory and Xilinx-HKUST Joint Laboratory at the Hong Kong University of Science and Technology, Hong Kong. His current research interests include NoC, multiprocessor SoC, optical interconnect, embedded system, computer architecture, low-power VLSI design, and hardware–software co-design.

Dr. Xu is the IEEE Distinguished Lecturer and was an ACM Distinguished Speaker. He authored or co-authored over 80 book chapters and papers in peer-reviewed journals and international conferences. He and his students received the Best Paper Award from the IEEE Computer Society Annual Symposium on VLSI in 2009, and the Best Poster Award from AMD Technical Forum and Exhibition in 2010. He co-authored a book entitled *Algorithms, Architecture, and System-on-Chip Design for Wireless Applications* (Cambridge University Press). He currently serves as an Area Editor of *NoC*, *SoC*, and GPU for ACM TRANSACTIONS ON EMBEDDED COMPUTING SYSTEMS and an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS. He served on the Steering Committees, Organizing Committees, and Technical Program Committees of many international conferences, including the DAC, ICCAD, CASES, ICCD, EMSOFT, CODES+ISSS, NOCS, RTCSA, and ASP-DAC.



Wei Zhang received the B.S. and M.S. degrees from the Harbin Institute of Technology, Harbin, China, in 1999 and 2001, respectively, and the Ph.D. degree from Princeton University, Princeton, NJ, USA, in 2009.

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