A Reflection on the TVLSI Editorial Process and the Announcement of a New Editor-In-Chief

WHEN I was appointed the Editor-In-Chief (EIC) of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS in January 2003, I was quite excited about the prospects and the impact I could make towards the TVLSI community, but at the same time, I was overwhelmed at the thought of the huge responsibility that is associated with the position. While there was a strong determination to take steps towards improving the Transactions, I wanted to also be careful to avoid any misstep that could have a negative impact on the Transactions. Four years have gone by and it has been a privilege and pleasure to serve the TVLSI community in that capacity for two terms with strong editorial boards. In the past four years, TVLSI has grown a lot in terms of the number of submissions, the annual page budget, frequency of issues, response times, etc. Thus, the IEEE TRANSACTIONS ON VLSI SYSTEMS is heading in the right direction.

As my term comes to an end, it is time to reflect on various aspects of the TVLSI editorial process. This past year, we saw a steep increase in the number of manuscript submissions both in the regular paper category and for the various special sections. When an author submits a paper, the first task is to make sure that the paper belongs to the focus thrusts of this Transactions. We often see, for example, a theoretical contribution in signal processing or a pure arithmetic paper or a device level paper submitted to TVLSI. When a manuscript is submitted through the manuscript central website to the TVLSI, it first goes to the administrative center for verification of format, appropriate author information, etc., after which the manuscript is sent to the EIC center. The EIC has to identify those submissions that fall outside the main focus areas of the journal and return them to the authors suggesting to submit their paper to a more appropriate journal.

An important task for the Editor-In-Chief is to assign the manuscript to the right Associate Editor. The Editor-In-Chief has to consider several issues, including area expertise, load distribution, conflict of interests, etc., while assigning the manuscript to an Associate Editor (AE). The AE's task is quite challenging. He has to send e-mails inviting reviewers and providing them with the title, author, and abstract information. Once the reviewer agrees to perform the review, the AE has to click on the manuscript in his web center to indicate the agreement by the reviewer after which manuscript central transfers the manuscript to the assigned reviewer's web center. Some AEs prefer automatic reminders which indicate when the time for submitting the review expires, while some prefer to send their own custom reminders. When a manuscript's processing has continued for more than three months without a decision recommendation, the administrative center sends out selective reminders to the reviewers. However, getting the manuscript reviewed and a recommendation made within this time period is the primary responsibility of the AE. The authors can only contact the EIC center or the administrative center for status information and until a recommendation of acceptance or rejection is sent to the author, the AE is unidentified to facilitate the AE to perform his task without being disturbed by the author. Also, this helps the EIC keep track of the status of manuscripts, in general. If the manuscript does not fall within the general focus of the journal and within the expertise of the editorial board, the identification of reviewers for the manuscript becomes difficult. Once the AE receives the reviews on a manuscript, he or she must read the reviews, read the paper at least once, and then make the recommendation. The manuscript then moves back to the EIC center for the EIC to make the final decision and transmit it to the corresponding author. At this point, for the manuscripts that are accepted, the final version of the paper is submitted in camera ready format as per the instructions in the acceptance letter. In the cases that need a major or minor revision, the review comments are attached to the paper. The reviews include information to be conveyed to the author as well as to the EIC with confidential comments, which are not seen by the author, to help make the final decision.

In most transactions, at this point, the author directly communicates the final camera ready manuscript to the IEEE publications office for scheduling, formatting, type setting, and printing. At this point, the backlog of camera ready manuscripts come into play and if the backlog is several months long, then the author will need to wait a long time before it appears in print. Some time in 2004 in TVLSI, we decided to ask the author to send the final manuscript to the EIC where the scheduling is done at the EIC center and the future issues, once scheduled, become the tentative table of contents to be published on the website. This way the author knows approximately when the accepted paper will appear in print. Also, the papers are subcategorized at the EIC center and, thus, the papers that relate to each other are somewhat scheduled to appear in the same issue for better visibility to the readers. In TVLSI, we have significantly reduced the backlog by improving the turnaround time for the manuscripts which is currently about two to three months. However, having a backlog of less than four months puts a lot of stress on the EIC center and the publications office since there is only a certain amount of time the publication office is allotted for type setting, proof reading by the author, reformatting, and in some cases, several rounds of communication to make the author reduce the manuscript to the specified page limits, etc. Over the past year, we have struggled with the small time period between the receipt of the final manuscript and its publication which, in turn, has resulted in a delay in the publication of the issue by a few weeks. The various statistics that affect the performance of the Transactions

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Row	NUMBER OF PAPERS:	2006	2005	2004	2003
1	Total number of papers submitted (new and revised)	782	539	402	440
2	Papers returned by EIC for scope reasons, poor quality, etc.	38	9	7	12
3	Papers to be peer reviewed (row 1 less row 2)	744	530	395	428
3a	Papers from Row 3 eventually rejected	163	184	95	108
3b	Papers from Row 3 in review process	299	7	1	0
3c	Papers from Row 3 being revised by authors, carried forward etc	128	227	171	223
3e	Papers from Row 3 that received final acceptance	154	112	128	97
4a	Average number of months from Author Submission to First Decision (use the date of author notification)	3.7	5	6	6
4b	Average number of months from Author Submission to Final Decision (use the date of author notification).	10.5	9.6	11.5	12.8
5	Average number of months from Author Submission of camera ready manuscript to Publication Date	3	3-4	4-6	5-7
6	Pages printed per year	1465	1468	1441	1200
7	No of issues per year	12	12	12	6
8	Journal impact factor (NA means not available yet)	NA	0.860	0.793	0.866
9	No. of citations	NA	1055	870	894
10	Downloads via IEEE Xplore	NA	168987	155030	111624

Region of author affiliation	2006 %	2005 %	2004 %	2003 %
Regions 1 – 6 (U.S.A.)	57	55	54	65
Region 7 (Canada)	7	12	6	4
Region 8 (Europe/Africa)	14	15	23	14
Region 9 (Central/South America)	<1	<1	0	0
Region 10 (Asia/Pacific)	18	14	16	14

are given in Table I. The statistics in Table I are automatically generated from the Manuscript Central report generator.

The whole process can run much smoother if a few minor details are paid attention to by all the different players in this process. The author, while submitting the manuscript, should indicate clearly all the following necessary information: include index terms that help in identifying the reviewers, indicate if the paper is for a specific special section, indicate names of reviewers that they feel they have a potential conflict of interest with, details of a related conference or workshop publication, and the details of what has been added on top of the previous conference publication, etc., in the notes to the EIC. It is not always possible for the EIC to identify conflicts of interest while assigning AEs or reviewers. While the reviewers fill out the forms, they should clearly indicate their recommendations, and back their decisions with arguments to be communicated to the AE and the authors. The important thing here is that the author should be able to clearly understand the basis for the rejection of the paper by reading the comments. The AE needs to summarize the reviewers' comments and make the recommendation by clearly indicating why a certain recommendation is being made. It needs to be understood that the decisions are made by considering the combined opinion of the independent referees and the recommendation of the AE. It is important for the AE to extract the essence of the reviewer comments and summarize them in an articulate fashion to convey the basis for acceptance or rejection of each particular paper.

Among the issues I would like to stress to the authors, one important issue is to strictly adhere to the page limits. A regular paper is allowed 10 transaction pages and the author is allowed 4 additional pages for which a mandatory page charge will apply. Thus, when the author formats the camera ready manuscript of a regular paper to be more than the ten allowed pages, it is automatically assumed that the author agrees to pay the additional page charges to the IEEE. Similarly, a brief is allowed four pages and the author is allowed a maximum of one extra page for which mandatory page charges will apply. The authors are requested to carefully adhere to these policies in order to avoid any delay or denial of publication at that stage.

Another important issue is that the authors make sure they cite all relevant works in the related work section of their paper and include all references in their paper. It is also very critical for TVLSI that the authors include the references to previous relevant papers published in this Transactions. We ask that the reviewers and the AEs pay particular attention to this aspect since the authors sometimes tend to unintentionally, or sometimes even intentionally, miss a few references to previous works. If we make sure that the previous works are cited appropriately, it will help in improving the impact factor and the ranking of the journal by scientific organizations. If the IEEE TRANSACTIONS ON VLSI SYSTEMS ranking improves, it benefits the entire community. The term "impact factor" is often misunderstood. Indicates the average number of times articles published in a specific journal in the previous two years were cited in a particular year.

The AEs can help improve the journal by monitoring the review process closely and making sure the decisions for an article are made in less than three months. It is not a good idea to invite more reviewers than needed for a specific manuscript. Typically, depending on the topic and the content, the AE may choose to invite three to five reviewers and make sure at least three reviewers have agreed to return the review within the given time. When the timeline given to the reviewers is passed, the reviewers who missed the deadline could receive a gentle e-mail reminder. If there is a problem, the AE could invite a new reviewer who will provide a prompt response. Unless the reviewer

database is constantly updated, it becomes difficult to conduct the review process in an efficient manner. Thus, one of the most important contributions of an AE is to recruit and add new reviewers to the database and inform the EIC or the editorial assistant when some of the reviewer information is outdated and the reviewer will need to be removed from the database. Therefore, I urge the AEs to contribute to the reviewer database and also, when they serve in other conference technical program committees, identify potential reviewers for the TVLSI database.

The success of the TVLSI depends on the review process involving the reviewers, associate editors, the associate EIC, and the EIC, who are all volunteers in spite of their own busy research schedules and professional obligations. The task of identifying good reviewers is the biggest challenge of this whole process. I would like to draw your attention to this factor. The manuscripts submitted to the TVLSI have anywhere from two to four authors on the average. For each paper submitted, at least three reviewers have to volunteer their time. For each manuscript submitted by an author, I challenge the author to commit to the responsibility of reviewing three papers for the journal. If that becomes the case, we will never run into a dearth for reviewers. It is only fair to expect an author to volunteer as much reviewing time as he expects to receive from the journal. Although it may be a little radical to implement such a policy, it is only fair to have such an expectation in terms of volunteering. I ask the authors to write to the EIC and the AEs in their areas of research indicating their willingness to review papers for this Transactions. It is such a spirit that will make the TVLSI an effective publication. Another way to contribute for the AEs is to identify outstanding and pioneering contributions presented in conferences and invite the authors to submit their work to the TVLSI in an informal manner. Although the papers will still go through the normal review process, such informal invitations tend to attract good quality submissions.

As my term ends, the incoming EIC will appoint a new set of AEs for the 2007–2008 term, in turn, forming his own editorial board. However, the current board of AEs will continue to serve until they complete the review process for all the manuscripts that have been assigned to them so far. The same applies for the guest editors of several special sections in the pipeline.

As it is the end of my second term as the EIC, it is time to thank and honor the outstanding voluntary work of these anonymous referees, who amidst their tremendous responsibilities associated with their own profession and jobs, have taken the time out to do this important duty. I would like to express my sincere thanks to each one of them. I had the privilege and honor to work with a large number of AEs who constituted two very strong editorial boards from 2003 to 2006. These are well accomplished outstanding professionals who have made significant contributions in their respective fields of research. I sincerely and respectfully express my gratitude to all of them. The Associate EIC, Dr. Srimat Chakradhar of NEC, has been a great source of support and experience. Whenever I ran into a difficulty, Chak was readily available to help me out. When I was unable to function last summer due to travel to India and personal circumstances, Chak took the responsibility of the TVLSI and worked in the background. I record my appreciation of his support and assistance throughout my two terms. My editorial assistant, Mr. Michael Pham's contributions were huge especially in the first two years as we started the new website to serve as the front end for the IEEE TRANSACTIONS ON VLSI SYSTEMS and the manuscript central portal. The person who is principally responsible for making sure that the IEEE TRANSACTIONS ON VLSI SYSTEMS printed issue comes out each month off the press is Ms. Mona Mittra at the IEEE. She is one of the best people to work with in this field of publishing. Her patience in dealing with the authors, her experience, and her diligence is terrific. Ms. Denise Hurley at the IEEE kept me informed of my duties towards the review committees and the budget issues and was a great help as I worked on getting the TVLSI page budget increased from 744 to 1000 to 1200 to 1400 during my tenure as the steering committee chair and later as the EIC. I would also like to record my thanks to Ms. Michelle Nixon and Mr. Richard Jannuzzi at the IEEE for their assistance with editorial and financial issues.

I would like to thank the steering committee members Dr. Eby Friedman, Dr. Wayne Wolf, Dr. Don Bouldin, Dr. Peter Pirsch, and Dr. Takayasu Sakurai for their support and encouragement as well as the IEEE Computer Society, the IEEE Circuits and Systems Society, and the IEEE Solid-State Circuits Society for their trust in me and for appointing me for two consecutive terms. I also owe my gratitude to several other individuals such as Dr. Vishwani Agrawal, Dr. Niraj Jha, Dr. Bing Sheu, Dr. Steve Kang, Dr. Massoud Pedram, Dr. Kasturi Rangachar, Dr. Michael Williams, Dr. Larry Hall, Dr. Oscar Garcia, Dr. Michael Lightner, and Dr. Amar Mukherjee for their advices, support, and consultations at various points of my term as EIC.

Finally, I come to the most important announcement. I am extremely delighted to announce that upon the unanimous recommendation of the TVLSI EIC search committee, the IEEE Circuits and Systems Society has selected Dr. Niraj Jha of Princeton University to serve as the next EIC, who will begin his official term in February 2007. There were several outstanding candidates for this position which indicates the strong status of the Transactions. Dr. Niraj Jha is an outstanding researcher and is extremely well known around the world for his huge contributions over more than two decades to the various aspects of VLSI systems. The TVLSI will enter a new era and will improve and continue to grow under the able leadership of Dr. Jha. He has served as an AE of the TVLSI for more than eight years and also has served on the editorial boards of several other reputed journals. His biography and photograph are given below.

NAGARAJAN (RANGA) RANGANATHAN, *Editor-in-Chief*

Department of Computer Science and Engineering
University of South Florida
Tampa, FL 33620 USA

Nagarajan "Ranga" Ranganathan (S'81–M'88–SM'92–F'02) received the B.E. (honors) degree in electrical and electronics engineering from Regional Engineering College, Tiruchirapalli, University of Madras, Madras, India, in 1983, and the Ph.D. degree in computer science from the University of Central Florida, Orlando, in 1988.

He is a Professor of Computer Science and Engineering at the University of South Florida, Tampa, where he has been since 1988. During 1998-1999, he was a Professor of Electrical and Computer Engineering at the University of Texas at El Paso. He has developed many special purpose VLSI systems for computer vision, image processing, pattern recognition, data compression and signal processing applications. He has published over 220 papers in reputed journals and conferences and is a co-owner of six U.S. patents with one pending. His research interests include VLSI system design, VLSI design automation, multi-metric optimization in VLSI computer-aided design (CAD), process variations, biomedical information processing, crisis management and homeland security applications, computer architecture, and parallel computing.

Dr. Ranganathan has served on the Editorial Boards for the following journals: *Pattern Recognition* (1993–1997), *VLSI Design* (1994–present), IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (1995–1997), IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS (1997–1999), and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY (1997–2000). He was the chair of the IEEE Computer Society Technical Committee on VLSI during 1997–2001. He served as the Steering Committee Chair of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS during 2001–2002 and served as the Editor-in-Chief for two consecutive terms from 2003 to 2006. He is a member of the IEEE Computer Society, IEEE Circuits and Systems Society, and the VLSI Society of India. He was elected as a Fellow of the IEEE in 2002 for his contributions to algorithms and architectures for VLSI systems. He received the USF Division of Sponsored Research Outstanding Research Achievement Award in 2002, the USF President's Faculty Excellence Award in 2003, USF Theodore-Venette Askounes Ashford Distinguished Scholar Award in 2003, and the Sigma Xi Scientific Honor Society Tampa Bay Chapter Outstanding Faculty Researcher Award in 2004. He was a co-recipient of three Best Paper Awards at the International Conference on VLSI Design in 1995, 2004, and 2006.

Niraj Jha (S'85–M'85–SM'93–F'98) received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, in 1981, the M.S. degree in electrical engineering from the State University of New York (SUNY) at Stony Brook, NY, in 1982, and the Ph.D. degree in electrical engineering from University of Illinois at Urbana-Champaign, in 1985.

He is a Professor of Electrical Engineering at Princeton University, Princeton, NJ. He has coauthored *Testing and Reliable Design of CMOS Circuits* (Kluwer, 1990), *High-Level Power Analysis and Optimization* (Kluwer, 1998), and *Testing of Digital Systems* (Cambridge Univ. Press, 2003). He has also authored six book chapters. He has authored or coauthored more than 300 technical papers. He is currently serving as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: REGULAR PAPERS, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and the *Journal of Low Power Electronics*. He has served as an Editor of the *Journal of Electronic Testing: Theory and Applications (JETTA)* in the past. He has served as the Guest Editor for the JETTA special issue on high-level test synthesis. He served as the Director of the Center for Embedded System-on-a-chip (SoC) Design funded by the New Jersey Commission on Science and Technology. He has received 11 U.S. patents. His research interests include nanotechnology, thermal analysis and optimization, computer-aided design of integrated circuits and systems, digital system testing, and computer security.

Dr. Jha is a Fellow of the Association for Computing Machinery (ACM). He is the recipient of the AT&T Foundation Award and NEC Preceptorship Award for research excellence, NCR Award for teaching excellence, and Princeton University Graduate Mentoring Award. He has co-authored seven papers which have won the Best Paper Award at ICCD'93, FTCS'97, ICVLSID'98, DAC'99, PDCS'02, ICVLSID'03, and CODES'06. A paper of his was selected for "The Best of ICCAD: A collection of the best IEEE International Conference on Computer-Aided Design papers of the past 20 years," and another by IEEE Micro as being among the best of 2005 Computer Architecture conference papers. He has served as the Program Chairman of the 1992 Workshop on Fault-Tolerant Parallel and Distributed Systems and the 2004 International Conference on Embedded and Ubiquitous Computing where he gave the keynote speech on nanotechnology in 2005.