Editorial

I T IS WITH great pleasure and deep sense of responsibility that I accept the position of the Editor-in-Chief of the IEEE TRANSACTIONS ON VERY LARGE SCALE (VLSI) SYSTEM (TVLSI). Previous Editors-in-Chief of this journal have worked tirelessly to bring this journal to the very top. Currently, TVLSI has a quick average review time, quality reviews, and fast acceptance-to-publication time due to an increased page budget added in the previous term. I had the privilege of working as the Associate Editor-in-Chief with my predecessor, Prof. Niraj Jha of Princeton, where significant effort was made to further improve TVLSI. It is the mission of the new board to maintain and further improve TVLSI in all respects.

The new board has been expanded by about 25% as compared to the previous board to enable even faster turnaround times and higher quality reviews. The areas of expertise of the board have been expanded and more Associate Editors have been added to areas where TVLSI receives a large number of submissions. The presence of top world class experts in the board in a diverse set of areas will enable precise allocation of papers to Associate Editors who are in exactly the same area as that of the paper, resulting in an appropriate assignment of reviewers and therefore higher quality reviews. The number of industry members was increased in the new board. About two-thirds of the previous board will continue with TVLSI in the new board and with the expansion of the board, about half the incoming board are new members.

I would like to thank the steering committee of TVLSI for their help with the board formation as well as their valuable advice and directions. I would also like to thank Ms. Mona Mittra, Ms. Michelle Gillespie, Ms. Sonal Parikh, Mr. Richard Jannuzzi, and other staff members for all their efforts to keep TVLSI running smoothly.

Last, but not least, I want to express my deep gratitude to the TVLSI Editorial Assistant, Ms. Stacey Weber Jackson, for her steady and extremely efficient service to TVLSI. I am happy that Ms. Weber Jackson has agreed to continue working as the Editorial Assistant of TVLSI during my term.

The biographies and photographs of the Associate Editors on the new editorial board are provided below.

PROF. YEHEA I. ISMAIL, *Editor-in-Chief*
Director of the Nanoelectronics Integrated
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Dr. Yehea Ismail (M'00–SM'10–F'11) received the B.Sc. degree and the M.S. degree from Cairo University, Cairo, Egypt, in 1993 and 1996, respectively, and the M.S. and Ph.D. degrees from the University of Rochester, Rochester, NY, in 1997 and 2000, respectively.

He is currently the director of the Nanoelectronics Integrated Systems Center (NISC), Northwestern University, Evanston, IL, and Nile University, Cairo, Egypt. The center is highly supported by Intel and was inaugurated by Craig Barrett, Intel's chairman of the board in 2008. He has published a large number of seminal papers in the top refereed journals and conferences and has coauthored several books and book chapters. He holds many patents in the area of high performance circuit and interconnect design and modeling.

Prof. Ismail has held several positions including the Associate Editor-in-Chief of the IEEE Transaction on VLSI (TVLSI) and the chair elect of the IEEE VLSI Technical Committee. He has served on the editorial boards of several prestigious journals and the committees of many top conferences since 2000. He was a recipient of several awards including the National Science Foundation Career Award, the IEEE CAS Outstanding Author Award, many Best Paper Awards, and Teaching Awards.

Massimo Alioto (M'01–SM'07) was born in Brescia, Italy, in 1972. He received the laurea degree in electronics engineering and the Ph.D. degree in electrical engineering from the University of Catania, Catania, Italy, in 1997 and 2001, respectively.

In 2002, he joined the Dipartimento di Ingegneria dell'Informazione (DII), University of Siena, Siena, Italy, as a Research Associate and in the same year as an Assistant Professor. In 2005, he was appointed Associate Professor of Electronics, and was engaged in the same faculty in 2006. In the summer of 2007, he was a Visiting Professor at EPFL—Lausanne, Switzerland. In 2009–2011, he is Visiting Professor with BWRC—University of California at Berkeley, Berkeley, CA, investigating on ultra-low power circuits and wireless nodes. Since 2001, he has been teaching undergraduate and graduate courses on advanced VLSI digital design, microelectronics, and basic electronics. He has authored or coauthored more than 160 publications on journals (55+, mostly IEEE Transactions) and conference proceedings. Two of them are among the 25 most downloaded TVLSI papers in 2007 (respectively, 10th and 13th). He is coauthor of the book *Model and Design of Bipolar and MOS Current-Mode Logic: CML, ECL, and SCL Digital Circuits* (Springer, 2005). His primary research interests include the modeling and the optimized design of CMOS high-performance, low-power and ultra low-power digital circuits, arithmetic and cryptographic circuits, interconnect modeling, design/modeling for variability-tolerant and low-leakage VLSI circuits, circuit techniques for emerging technologies. He is the director of the Electronics Lab at University of Siena (site of Arezzo).

Prof. Alioto is a member of the HiPEAC Network of Excellence. He is the Chair of the "VLSI Systems and Applications" Technical Committee of the IEEE Circuits and Systems Society, for which he is also Distinguished Lecturer. He is regularly invited to give talks and tutorials to academic institutions, conferences, and companies throughout the world. He has served as a member of various conference technical program committees (ISCAS, ICCD, PATMOS, ICM, ECCTD, CSIE) and Track Chair (ISCAS, ICCD, ICECS, ICM). He was the Technical Chair of the conference ICM 2010. He serves as Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, as well as of the *Microelectronics Journal*, the *Integration—The VLSI Journal*, the *Journal of Circuits, Systems, and Computers*, the *Journal of Low Power Electronics and Applications*, and the *ACM Transactions on Design Automation of Electronic Systems*. He is Guest Editor of the Special Issue "Advances in Oscillator Analysis and Design" of the *Journal of Circuits, Systems, and Computers* (2010), and Technical Program Chair for the *ICM 2010* Conference.

Elad Alon received the B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 2001, 2002, and 2006, respectively.

In January 2007, he joined the University of California at Berkeley, Berkeley, as an Assistant Professor of electrical engineering and computer sciences, where he is now a codirector of the Berkeley Wireless Research Center (BWRC). He has held positions at Sun Labs, Intel, AMD, Rambus, Hewlett Packard, and IBM Research, where he worked on digital, analog, and mixed-signal integrated circuits for computing, test, and measurement, and high-speed communications.

Dr. Alon was a recipient of the IBM Faculty Award in 2008, the 2009 Hellman Family Faculty Fund Award, and the 2010 UC Berkeley Electrical Engineering Outstanding Teaching Award. His research focuses on energy-efficient integrated systems, including the circuit, device, communications, and optimization techniques used to design them.

Mohab Anis (S'98–M'03–SM'09) received the B.S. degree (with honors) in electronics and communication engineering from Cairo University, Cairo, Egypt, in 1997, and the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Waterloo, Waterloo, ON, Canada, in 1999 and 2003, respectively. He also holds an M.B.A. degree with a concentration in entrepreneurship and innovation and an M.S. degree with a concentration in management of technology.

He is currently an Associate Professor with the Department of Electronics Engineering, The American University in Cairo, Cairo, Egypt. Previously, he was a Tenured Associate Professor with the University of Waterloo, where he is now an Adjunct. He has authored/coauthored over 100 papers in international journals and conferences and is the author of three books: *Multi-Threshold CMOS Digital Circuits-Managing Leakage Power* (Kluwer, 2003), *Low-Power Design of Nanometer FPGAs: Architecture and EDA* (Morgan Kaufmann, 2009), and *Nanometer Variation-Tolerant SRAM: Circuits and Statistical Design for Yield* (Springer, 2011). His current research interests include integrated circuit design and design automation for very large scale integration systems in the nanometer regime.

Dr. Anis is an Associate Editor of the *ACM Transactions on Design Automation of Electronic Systems*, the *Microelectronics Journal*, the *Journal of Circuits, Systems and Computers*, and the *ASP Journal of Low Power Electronics*. He is an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS. From 2008 to 2009, he was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS. He is a member of the program committees for several IEEE and ACM conferences, and is the General Chair of the 2010 International Conference on Microelectronics. He was the recipient of the 2009 Early Research Award from Ontarios Ministry of Research and Innovation, the 2004 Douglas R. Colton Medal for Research Excellence in recognition of his excellence in research, leading to new understanding and novel developments in microsystems in Canada, and the 2002 International Low-Power Design Contest. He is an advocate of technological innovation, for which he founded INNOVETY LLC, Egypt, a management consulting and software development firm that focuses on innovation management. In addition, he is the Executive for Strategic Programs at Egypt's Technology Innovation and Entrepreneurship Centre where he overlooks Egypt's innovation strategy in the ICT sector.

Dr. Tawfik Arabi received the B.S.E.E. degree from American University of Beirut (AUB), Beirut, Lebanon, in 1985 and the Ph.D. degree from Syracuse University, Syracuse, NY, in 1991.

He is the founder and director of Intel's Middle East Energy Efficiency Research Initiative. He is the author of over 100 Journal and conference publications. He supported and directed research programs between Intel and several leading universities in the U.S. and abroad.

Dr. Arabi was a recipient of many Intel and IEEE Awards including six Intel Achievement Award (Intel most prestigious given by the executive staff to only a handful of teams every year).

Iris Bahar received the B.S. and M.S. degrees in computer engineering from the University of Illinois, Urbana-Champaign, and the Ph.D. degree in electrical and computer engineering from the University of Colorado, Boulder.

From 1987 to 1992, she worked for Digital Equipment Corporation (in what is now the Intel Hudson facility), and was part of the NVAX Microprocessor Design Team. Since 1996, she has been with the Division of Engineering, Brown University, Providence, RI, where she is currently an Associate Professor. Her research interests include power-aware computer architecture; computer-aided design for synthesis, verification, and low-power applications; and design, test, and reliability issues for nanoscale systems.

Valeriu Beiu (S'92–M'95–SM'96) received the M.Sc. degree in computer engineering from the "Politehnica" University of Bucharest, Bucharest, Romania, in 1980, and the Ph.D. degree with *summa cum laude* in electrical engineering from the Katholieke Universiteit Leuven, Leuven, Belgium, in 1994.

Upon graduation, for two years he has been working on high-speed CPUs and FPUs with the Research Institute for Computer Techniques, Bucharest, Romania, prior to returning to the "Politehnica" University of Bucharest. Since 1991, he has been on leave of absence as follows: Katholieke Universiteit Leuven (1991–1994, Leuven, Belgium), King's College London (1994–1996, London, U.K.), and Los Alamos National Laboratory (1996–1998, Los Alamos, NM). In 1998, he cofounded RN2R (Dallas, TX) a VLSI IP startup company, and was its Chief Technical Officer (1998–2001). In 2001, he joined the School of Electrical Engineering and Computer Science, Washington State University, Pullman, and in 2005 he became Visiting Professor with the School of Computing and Intelligent Systems, University of Ulster, Ulster, U.K. Since 2006, he has been the Associate Dean for Research and Graduate Studies, Faculty of Information Technology, United

Arab Emirates University, Al Ain, Abu Dhabi, UAE. He holds 11 patents, has given over 150 invited talks, and authored over 170 technical papers in journals and conferences. He has authored six chapters (out of which five invited), and is working on one book on emerging brain-inspired nano-architectures, and another one on the VLSI complexity of discrete neural networks. His main research interests include VLSI-efficient designs (low-power and highly reliable) and emerging nano-architectures (massively parallel, fault-tolerant, communication starved, adaptive/reconfigurable), as well as their optimal implementations inspired by neural networks and biological arrays.

Dr. Beiu was a recipient of five fellowships including: Fulbright (1991), Human Capital and Mobility (1994–1996) with King's College London ("Programmable Neural Arrays" Project), Director's Funded Postdoc (1996–1998) with Los Alamos National Laboratory ("Field Programmable Neural Arrays" Project, under the Deployable Adaptive Processing Systems initiative), and Fellow of Rose Research (1999–2001). He was the principal investigator (PI) or co-PI of over 60 research contracts totaling over US\$ 22M. He was a recipient of 7 Best Paper Awards. He is a founding member of the European Neural Network Society (ENNS), and a member of: the International Neural Network Society (INNS), the Association for Computing Machinery (ACM), and the Marie Curie Fellowship Association (MCFA). He was a member of the SRC-NNI Working Group on Novel Nano-architectures (2003–2006), of the IEEE CS Task Force on Nanoarchitectures (since 2005), and of the IEEE Emerging Technologies Group on Nanoscale Communications (since 2010). He has organized over 50 conferences/workshops and chaired over 40 conference sessions, was the Program Chairman of the IEEE Los Alamos Section (1997), was an Associate Editor of the IEEE TRANSACTIONS ON NEURAL NETWORKS (2005–2008), and since 2010 is an Associate Editor of the *Nano Communication Networks* (Elsevier).

Sanjukta Bhanja received the Bachelor degree in electrical engineering from Jadavpur University, Calcutta, in 1991, the Masters degree from Indian Institute of Science, Bangalore, India, in 1994, and the Ph.D. degree in computer science and engineering from the University of South Florida (USF), Tampa, in 2002.

She is currently an Associate Professor with the Department of Electrical Engineering, USF. Her primary research focus is in non-CMOS nano-computing, exploring novel state variables, alternate computing paradigm with heterogeneous devices, VLSI design automation with emphasis on data-driven uncertainties, trade-off of error, power, and reliability at various levels of design abstractions. She has published over 60 publications in top-tier peer-reviewed journal and conferences in VLSI and nano-electronics area.

Dr. Bhanja is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. She has served on the Technical Program Committee of various IEEE and ACM conferences. She is currently the "Emerging Technology track" co-chair in IEEE DATE'11 and has served as Technical Program Co-Chair of IEEE ISVLSI, ACM GLSVLSI and as General Co-Chair of ACM GLSVLSI. She was a recipient of the New Researcher Award from the University of South Florida in 2002, the NSF CAREER Award (2007–2012), USF Tau Beta Pi "Outstanding Engineering Faculty Researcher" Award in 2007, the USF 2008 "Outstanding Faculty Research Achievement Award," the 2010 Florida Education Foundation (F.E.F) William Jones Outstanding Mentor Award, and the USF 09/10 Outstanding Undergraduate Teaching Award.

Chirn Chye Boon (M'09–SM'10) received the B.E. (Hons.) degree in electronics and the Ph.D. in electrical engineering from Nanyang Technological University (NTU), Singapore, in 2000 and 2004, respectively.

In 2005, he joined NTU as a Research Fellow and became an Assistant Professor in the same year. Before that, he was with Advanced RFIC, where he worked as a Senior Engineer. He specializes in the areas of radio frequency (RF) and MM-wave circuits and systems design for Biomedical and Communications applications. He has coauthored over 49 refereed publications and several patents in the fields of RF and MM-wave. He is a coauthor of the book *Design of CMOS RF Integrated Circuits and Systems* (World Scientific Publishing, 2010).

Dr. Boon serves as a committee member for various conferences and is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He is the Programme Director for RF and MM-wave research in the SG\$50 millions research centre of excellence, VIRTUS (NTU) since March 2010. He is the Principal/Co-Principal Investigator for research grants of more than SG\$3 250 000.

Chaitali Chakrabarti received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, and the M.S. and Ph.D. degrees in electrical engineering from the University of Maryland, College Park.

She has been a Professor with Arizona State University (ASU), Tempe, since 1990. Her research interests include the areas of specialized architectures for signal processing and wireless communications, software defined radio, algorithm-architecture co-design, low power algorithms, and energy-efficient embedded system design including those powered by fuel cells.

Dr. Chakrabarti is a member of the Consortium of Embedded Systems and the Sensor, Signal, and Information Processing Center, ASU. She was a recipient of the Research Initiation Award from the National Science Foundation in 1993, a Best Teacher Award from the College of Engineering and Applied Sciences in 1994, and the Outstanding Educator Award from the IEEE Phoenix section in 2001. She has been on the program committees of ICASSP, ISCAS, SiPS, ASAP, DAC, and ISLPED. She served as an Associate Editor (AE) of the IEEE TRANSACTIONS ON SIGNAL PROCESSING (1999–2005) and also as an Associate Editor of the *Journal of VLSI Signal Processing Systems*. She is the Chair of the Technical Committee of Design and Implementation of Signal Processing Systems, IEEE Signal Processing Society.

Chip-Hong Chang (S'92–M'98–SM'03) received the B.Eng. (Hons.) degree from the National University of Singapore, Singapore, in 1989, and the M.Eng. and Ph.D. degrees from Nanyang Technological University (NTU), Singapore, in 1993 and 1998, respectively.

He served as a Technical Consultant in industry prior to joining the School of Electrical and Electronic Engineering (EEE), NTU, in 1999, where he is currently an Associate Professor. He holds joint appointments with the university as an Assistant Chair of Alumni of the School of Electrical and Electronic Engineering (EEE) since June 2008, the Deputy Director of the Center for High Performance Embedded Systems since 2000, and the Program Director of the Center for Integrated Circuits and Systems from 2003 to 2009. His current research interests include low power arithmetic circuits, residue number system, digital filter design, and digital watermarking for VLSI intellectual property protection. He has coedited one book, published three book chapters, and over 170 research papers in refereed international journals and conferences.

Dr. Chang has served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS in 2010–2011 and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS since 2011, Editorial Advisory Board Member of the *Open Electrical and Electronic Engineering Journal* since 2007 and Editorial Board Member of the *Journal of Electrical and Computer Engineering* since 2008. He also served as a Guest Editor for the special issue of the *Journal of Circuits, Systems, and Computers* in 2010, and in several international conference advisory and technical program committees. He is a Fellow of the IET. He was the corecipient of two paper awards at PrimeAsia 2010 and the finalist of the Best Paper Award at VLSI'95.

Jonathan Chang (SM'06–M'93) received the B.S. degree in electrical engineering from National Taiwan University, Taiwan, in 1990, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1994 and 1998, respectively.

He joined Intel Corporation, Santa Clara, CA, in 1998 and since has been engaged in the design of several high-performance microprocessors with emphasis in large, high-speed, low power cache design. He was a Principal Engineer in the area of cache design in Enterprise Microprocessor Group. He joined TSMC, Hsin-Chu, Taiwan, in 2010 as a deputy director and is responsible for high speed embedded SRAM products. He is currently among the technical committee of 2011 VLSI symposium on circuits. He has published over 20 technical papers in IEEE conferences or journals.

Robert Chen-Hao Chang (S'91–M'95–SM'09) received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1987 and 1989, respectively, and the Ph.D. degree in electrical engineering from University of Southern California (USC), Los Angeles, in 1995.

In 1996, he joined the faculty of the Department of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan, where he is currently a Professor. He served as the Director of Meng Yao Chip Center from 2000 to 2004, the Director of Center for Research and Development of Engineering Technology of the College of Engineering from 2005 to 2006, and Chairman of the Electrical Engineering Department from 2006 to 2008. He has published over 90 technical journal and conference papers. His research interests include mixed-signal IC design, power management IC design, low-power circuits design, and baseband circuits design.

Dr. Chang was a recipient of the National Science Council Research Award in 1997 and 1998, the Distinguished Teaching Award, the Outstanding Research Project Award, and the Distinguished Teacher Evaluation Award from National Chung Hsing University in 2004, 2006, and 2009, respectively. He was listed in the Marquis Who's Who in the World 2000. He is a member of Tau Beta Pi. He has been a Member of VLSI Systems and Applications Technical Committee, IEEE Circuits and Systems Society since 2004. He is an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and the Chair of IEEE CASS Taipei Chapter. He also served as Technical Program Committee Member for many conferences.

Dr. Deming Chen received the B.S. degree in computer science from University of Pittsburgh, Pittsburgh, PA, in 1995, and the M.S. and Ph.D. degrees in computer science from University of California at Los Angeles, in 2001 and 2005, respectively.

He worked as a Software Engineer between 1995–1999 and 2001–2002. He has been an Assistant Professor with the Electrical and Computer Engineering Department, University of Illinois, Urbana-Champaign, since 2005. He is a Research Assistant Professor with the Coordinated Science Laboratory and an affiliate Assistant Professor with the Computer Science Department. His current research interests include high-level synthesis, nano-systems design and nano-centric CAD techniques, FPGA synthesis and physical design, microarchitecture and SoC design under parameter variation, and reconfigurable computing.

Dr. Chen is a technical committee member for a series of conferences and symposia, including FPGA, ASPDAC, ICCD, ISQED, DAC, ICCAD, and DATE, etc. He also served as session chair, panelist, panel organizer, or moderator for some of these and other conferences. He is the TPC subcommittee chair for ASPDAC'09–2011 and the CAD Track co-chair for ISVLSI'09 and ISCAS'10–2011. He is the program chair for SLIP'11. He is an Associated Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (TVLSI), IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS (TCAS-I), *Journal of Circuits, Systems and Computers* (JCSC), and *Journal of Low Power Electronics* (JOLPE). He was a recipient of the Achievement Award for Excellent Teamwork from Aplus Design Technologies in 2001, the Arnold O. Beckman Research Award from UIUC in 2007, the NSF CAREER Award in 2008, the ASPDAC'09 Best Paper Award, and the SASP'09 Best Paper Award. He is included in the List of Teachers Ranked as Excellent in 2008. He received the ACM SIGDA Outstanding New Faculty Award in 2010.

Poki Chen (M'05) was born in Chia-Yi, Taiwan, in 1963. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 1985, 1987, and 2001, respectively.

During 1998–2001 and 2001–2006, he was a Lecturer and an Assistant Professor correspondingly with the Electronic Engineering Department, National Taiwan University of Science and Technology (NTUST), Taiwan. He is currently an Associate Professor with the same department. Since 2010, he was selected as the director of System-on-Chip Research Center, NTUST. His research interests include analog/mixed-signal integrated circuits and systems with a special interest focused on time-domain signal processing circuits, such as time-domain smart temperature sensor, time-to-digital converter, digital pulse generator, digital pulse width modulator, and duty cycle corrector. He is also interested in creating innovative analog applications for FPGA platforms, such as FPGA smart temperature sensor, FPGA digital-to-time, and time-to-digital converters.

Pasquale Corsonello was born in Cosenza, Italy, on May 4, 1964. He received the Master degree in electronics engineering from the University of Naples "Federico II", Naples, Italy, in 1988.

He joined the Institute of Research on Parallel Computers, National Council of Research of Italy, Naples, Italy, where he was working on the design and modelling of electronic transducers for high precision measurement, receiving a post-graduate two-years grant. In 1992, he joined the Department of Electronics, Computer Science, and Systems, University of Calabria, Rende, Italy, as a Research Associate. In 1997, he was appointed an Assistant Professor of electronics with the Department of Electronics Engineering and Applied Mathematics, University of Reggio Calabria, Reggio Calabria, Italy, where he also served as the Director of the Microelectronics Laboratory. In 2001, he was appointed an Associate Professor of electronics and Chair of the Ph.D. Program in electronics engineering at the University of Reggio Calabria. In the summer 2004, he was a Visiting Researcher with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY. In 2005, he was appointed as Adjunct Associate Professor with the same Department. He is currently an Associate Professor of electronics with the Department of Electronics, Computer Science, and Systems of the University of Calabria, Rende, Italy. His main research interests include high-performance arithmetic circuits, low-power design, VLSI architecture for image processing and multimedia, reconfigurable systems. He has coauthored over 120 technical papers and holds two patents in these fields. One of these papers is among the 25 most downloaded TVLSI papers in 2007.

Prof. Corsonello was a recipient of the Best Paper Award at the 2010 IEEE Conference on Advances in Circuits, Electronics and Micro-Electronics, CENICS 2010. He has also received several grants from both private industries and government agencies for projects in these areas. He serves on technical committees of several VLSI conferences and as a peer reviewer for several VLSI journals. He is an Associate Editor of the *Journal of Low Power Electronics and Applications*.

Vivek De (F'11) received the Bachelor's degree from the Indian Institute of Technology, Madras, India, the Master's degree from Duke University, Durham, NC, and the Ph.D. degree from Rensselaer Polytechnic Institute, Rensselaer, NY, all in electrical engineering.

He is an Intel Fellow and Director of Circuit Technology Research with Intel Labs, Hillsboro, OR. He joined Intel in 1996 as a Staff Engineer in Intel's Circuits Research Lab (CRL). Since that time, he has led research teams in CRL focused on developing advanced circuits and design techniques for low-power and high-performance processors. In his current role as Director of CRL, he is responsible for providing strategic directions for research in future circuit technologies and aligning Intel's circuit research with technology scaling challenges. He has 193 publications in refereed international conferences and journals, and 172 patents, with 31 more patents filed (pending).

Dr. De was a recipient of an Intel Achievement Award for his contributions to a novel integrated voltage regulator technology.

Sang H. Dhong (M'76–SM'99–F'01) received the B.S.E.E. degree from the Korea University, Seoul, Korea, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley, Berkeley.

He is a Director, primarily responsible for embedded CPU/GPU design capability enhancement, in Design and Technology Platform, Taiwan Semiconductor Manufacturing Company (TSMC), Ltd., Taiwan, since 2009. He was a Senior Fellow at AMD from 2007 to 2009. He was an IBM Distinguished Engineer, a member of IBM Academy of Technology, and an IBM Master Inventor. He holds 140 U.S. patents as well as more than 50 technical publications/presentations. He joined IBM's Research Division, Yorktown Heights, NY, in 1983 as a research staff member where he was involved in the research and development of silicon processing technology, mainly bipolar devices and reactive-ion etching (RIE). From 1985 to 1992, he was engaged in research and development of DRAM cell structures, architectures, and designs, spanning over five generations of IBM DRAMs, from 1 Mb DRAMs to 256 Mb DRAMs. The key contributions in this area are high-speed DRAMs, low-power DRAMs, and NMOS-access transistor trench DRAM cells. After spending three years in development of one of IBM's PowerPC microprocessors as a Branch/Icache circuit team leader of 15 designers, he worked on a simple but fast processor core

based on the PowerPC architecture and on high-speed embedded DRAM (eDRAM) in the Austin Research Lab, IBM Research Division, leading, managing, and growing the high-performance VLSI design group to a peak of 25 people from 1995 to 1999. The work resulted in setting a major milestone for the microprocessor industry by prototyping1-GHz PowerPC processors. Also, the work on the high-speed eDRAM provided the justification for the logic-based eDRAM foundry/ASIC technology offering by IBM as well as the design basis for eDRAM macros of DRAM-like density with SRAM-like high speed. Since becoming the chief technologist of the Austin Research Lab, in 1999, he worked on three areas: fast low-power embedded PowerPC, super-pipelined multi-gigahertz PowerPC servers, and high-speed eDRAM. In 2000, he joined the Sony-Toshiba-IBM (STI) Design Center as one of the key leaders, primarily concentrating on a 11-FO4 coprocessor design, streaming process (SPE). As the partition leader of SPE team, he defined, executed, and delivered the technology, circuits, and latch styles, floor plan, and basic lower-power micro-architecture and led technically a multidiscipline team of 70 or more engineers. Until February 2007, he was the chief hardware engineer/SPE partition lead, being responsible for productization of BE chip from the STI center side. In this role, his major focus is on power-frequency yield tradeoff, interacting and guiding PE, manufacturing, and design teams in a matrix organization of more than 100 engineers. This work played one of the most crucial roles in a successful launch of PS-3 Sony PlayStation in late 2006.

Robert Dick (S'95–M'02) received the B.S. degree from Clarkson University, Potsdam, NY, in 1996, and the Ph.D. degree from Princeton University, Princeton, NJ, in 2002.

He is an Associate Professor with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor. He worked as a Visiting Professor with the Department of Electronic Engineering, Tsinghua University, in 2002, as a Visiting Researcher at NEC Labs America in 1999, and was on the faculty of Northwestern University from 2003 to 2008. He has published in the areas of embedded operating systems, data compression, embedded system synthesis, dynamic power management, low-power and temperature-aware integrated circuit design, wireless sensor networks, human perception aware computer design, reliability, embedded system security, and behavioral synthesis.

Prof. Dick was a recipient of an NSF CAREER Award and won his department's Best Teacher of the Year Award in 2004. In 2007, his technology won a Computerworld Horizon Award and his paper was selected as one of the 30 in a collection of high-impact DATE papers appearing during the past 10 years. His 2010 work won a Best Paper Award at DATE. He is an Associate Editor of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, a Guest Editor for *ACM Transactions on Embedded Computing Systems*, was selected as Technical Program Committee Co-Chair of the 2011 International Conference on Hardware/Software Codesign and System Synthesis, and serves on the technical program committees of several embedded systems and CAD/VLSI Conferences.

Nikil D. Dutt (F'08) received the Ph.D. degree in computer science from the University of Illinois at Urbana-Champaign, Urbana-Champaign, in 1989.

He is currently a Chancellor's Professor with the University of California, Irvine, with academic appointments in the Computer Science and Electrical Engineering and Computer Science Departments. His research interests include embedded systems design automation, computer architecture, optimizing compilers, system specification techniques, and distributed embedded systems.

Dr. Dutt was a recipient of Best Paper Awards at CHDL89, CHDL91, VLSIDesign2003, CODES+ISSS 2003, CNCC 2006, and ASPDAC-2006. He was an ACM SIGDA Distinguished Lecturer during 2001–2002, and an IEEE Computer Society Distinguished Visitor for 2003–2005. He has served on the steering, organizing, and program committees of several premier CAD and Embedded System Design conferences and workshops, including ASPDAC, CASES, CODES+ISSS, DATE, ICCAD, ISLPED, LCTES, RTAS, and RTSS. He serves or has served on the advisory boards of ACM SIGBED and ACM SIGDA and is Vice-Chair of IFIP WG 10.5.

Maged Ghoneima (M'97) received the B.Sc. degree in electronics and communications engineering with Honors and the M.Sc. degree in electronics from Ain Shams University, Cairo, Egypt, in 1997 and 2000, and the Ph.D. degree in computer engineering from Northwestern University, Evanston, IL, in 2006.

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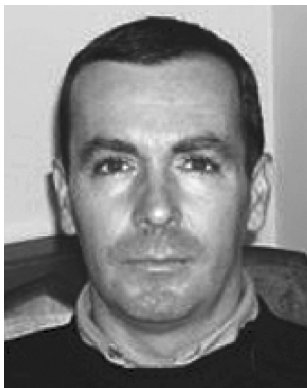
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Dr. Joshi was a recipient of an Outstanding Technical Achievement Award for his contributions to IBM microprocessor designs. He has won 50 invention plateau achievement awards from IBM and won two divisional patent portfolio awards for cross-licensing and utilization of his patents in the IBM products. He received three *Corporate Patent Portfolio Awards* from IBM for licensing contributions. He received the Lewis Winner Award in 1992 for an outstanding paper he coauthored at the International Solid State Circuit Conference. He was instrumental in starting interconnect workshop in early 1980s. He chaired advanced interconnect conferences sponsored by MRS and served as an editor of the proceedings. He is a fellow of ISQED and serves as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He served on committees of ISLPED (International Symposium Low Power Electronic Design) IEEE VLSI Design, IEEE International SOI Conference ISQED Program committees.

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Dr. Karnik was a recipient of an Intel Achievement Award for the pioneering work on integrated power delivery. He has presented several invited talks and tutorials, and has served on five Ph.D. students' committees. He was a member of ISSCC, DAC, ICCAD, ICICDT, and ISQED program committees and JSSC, TCAD, TVLSI, and TCAS review committees. He was the General Chair of ASQED'10, ISQED'08, ISQED'09, and ICICDT'08. He is an ISQED Fellow and a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.

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He performed research on mixed-signal thermal inkjet integrated circuits with Xerox Corporation, Webster, NY, in 2000. During summers 2001 and 2002, he was with Intel Microprocessor Research Laboratories, Hillsboro, OR, where he was responsible for the modeling and design of high frequency monolithic power supplies. During summer 2008, he was a Visiting Professor with the Chuo University, Tokyo, Japan. He served as an Assistant Professor with the Department of Electrical and Computer Engineering, University of Wisconsin, Madison, from August 2004 to August 2008. He has been an Assistant Professor with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, China, since August 2008. His current research interests include the areas of nanoelectronics, low power and robust integrated circuit design, and gigascale 3-D system-on-chip integration with nanoscale devices and interconnect. He has over 100 publications and six issued and two pending patents in the areas of high performance integrated circuits and novel semiconductor devices. He is the author of the book *Multi-Voltage CMOS Circuit Design* (Wiley, 2006).

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Mohammad M. Mansour (S'10) received the B.E. degree with distinction and the M.E. degree from the American University of Beirut (AUB), Beirut, Lebanon, in 1996 and 1998, respectively, both in computer and communications engineering, and the M.S. degree in mathematics and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign (UIUC), Urbana, in 2002 and 2003, respectively.

He is currently an Associate Professor of electrical and computer engineering with the Electrical and Computer Engineering Department, AUB, Beirut, Lebanon. From December 2006 to August 2008, he was on research leave with QUALCOMM Flarion Technologies, Bridgewater, NJ, where he worked on modem design and implementation for 3GPP-LTE, 3GPP-UMB, and peer-to-peer wireless networking PHY layer standards. From 1998 to 2003, he was a Research Assistant with the Coordinated Science Laboratory (CSL), UIUC. He joined the faculty at AUB in Fall 2003. During the summer of 2000, he worked at National Semiconductor Corporation, San Francisco, CA, with the Wireless Research Group. In 1997, he was a Research Assistant with the Electrical and Computer Engineering Department, AUB, and in 1996, he was a Teaching Assistant at the same department. His research interests include VLSI design and implementation for embedded signal processing and wireless communications systems, coding theory and its applications, digital signal processing systems, and general purpose computing systems.

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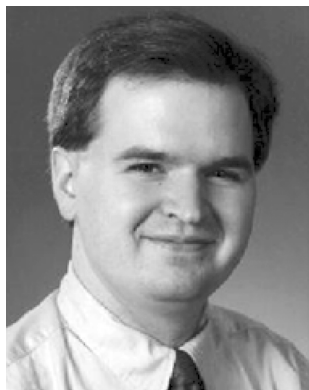
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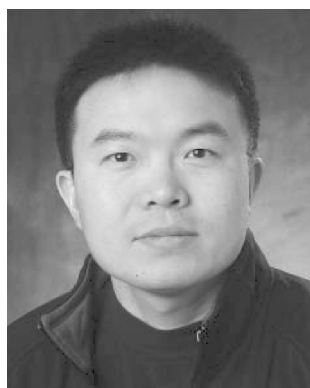
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