Editorial

IT is with deep humility and a sense of great responsibility that I take on the position of Editor-in-Chief (EIC) of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (TVLSI). I would like to thank the TVLSI steering committee headed by Dr. Eby Friedman and consisting of Dr. Don Bouldin, Dr. Peter Pirsch, Dr. Nagarajan Ranganathan, Dr. Takayasu Sakurai, and Dr. Wayne Wolf, for putting their faith in me for this position.

I would like to thank the previous EIC, Dr. Ranganathan, for his dedication to constantly improving TVLSI's quality over his two terms and so ably steering TVLSI through significant changes. He leaves TVLSI behind in excellent shape. His editorial in the January 2007 issue provides the metrics that show the tremendous strides made in the last four years under his leadership, even as the number of submitted papers roughly doubled in that timeframe. He has been a constant source of help and encouragement during this transition period, and has kindly agreed to continue discharging the duties of the EIC for several weeks beyond the end of his tenure in order to quickly bring me up to speed with all the EIC duties, which has made this transition much easier than I expected.

I would next like to thank Prof. Yehea Ismail who has agreed to take up the position of Associate EIC. He is very well known for his work on physical design of VLSI circuits. He has served as an associate editor (AE) of TVLSI for many years. He will help with sharing the EIC burden when needed, dealing with papers involving conflicts of interest, and setting new TVLSI policies to make the process more efficient.

TVLSI salutes the previous editorial board members who have selflessly devoted their time and energy to making the whole process of requesting reviewers, assigning papers to those who agree, reminding reviewers who may be late, and making decisions, run very smoothly. These members have agreed to continue dealing with manuscripts assigned to them until a final decision is taken, in order to provide continuity from one board to the next. TVLSI is very lucky to have a distinguished set of researchers who have agreed to serve on the board for the next two years. Their biographies and photographs are presented after

this editorial. In light of the doubling of the number of submitted papers to TVLSI over the last four years, we have increased the size of the Editorial Board to 29. This will lighten the burden on individual AEs, allowing them to make quicker decisions.

The quality of TVLSI depends heavily on the reviewers who take time from their busy schedules to provide detailed and prompt reviews, and the authors who submit their significant manuscripts to it. We aim to provide at least three reviews for most manuscripts. Thus, it is our request that authors be willing to review at least three manuscripts for each one they submit. It will be our aim to strive for an average submission-to-decision time of around three months. It is very important for research to be published in a timely fashion. This will require a very close collaboration among the EIC, AEs, and reviewers. It is also very important for authors to revise their manuscripts within a few weeks so that the manuscript is not outdated by the time it appears in TVLSI. This will improve the impact factor of the journal and attract even more high-quality manuscripts in the future.

Bringing out TVLSI issues on time requires a set of dedicated staff members. I would like to thank Ms. Mona Mittra, Ms. Michelle Nixon, Ms. Sonal Parikh, Mr. Richard Jannuzzi, and other staff members for being on top of the editorial, administrative, and financial issues. Without their hard work behind the scenes, TVLSI would not be what it is.

I would also like to introduce Ms. Stacey Weber Jackson as the new editorial assistant. In this role, she has already been a great asset to me in terms of promptly bringing submitted papers to my attention, responding to queries from authors, updating the response letters, enabling the new AEs to quickly start discharging their duties, removing outdated e-mail addresses from the database, etc. Without her attention to detail, TVLSI would not be as efficient as it should be.

Finally, we welcome advice from the TVLSI community on how we could serve the community better.

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Niraj K. Jha (S'85–M'85–SM'93–F'98) received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, in 1981, the M.S. degree in electrical engineering from the State University of New York (SUNY) at Stony Brook, NY, in 1982, and the Ph.D. degree in electrical engineering from University of Illinois at Urbana-Champaign, in 1985.

He is a Professor of Electrical Engineering at Princeton University, Princeton, NJ. He has coauthored *Testing and Reliable Design of CMOS Circuits* (Kluwer, 1990), *High-Level Power Analysis and Optimization* (Kluwer, 1998), and *Testing of Digital Systems* (Cambridge Univ. Press, 2003). He has also authored six book chapters. He has authored or coauthored more than 300 technical papers. He is currently serving as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and the *Journal of Low Power Electronics*. He has served as an Editor of the *Journal of Electronic Testing: Theory and Applications (JETTA)* in the past. He has served as the Guest Editor for the JETTA special issue on high-level test synthesis. He served as the Director of the Center for Embedded System-on-a-chip (SoC) Design funded by the New Jersey Commission on Science and Technology. He has received 11 U.S. patents. His research interests include nanotechnology, thermal analysis and optimization, computer-aided design of integrated circuits and systems, digital system testing, and computer security.

Dr. Jha is a Fellow of the Association for Computing Machinery (ACM). He is the recipient of the AT&T Foundation Award and NEC Preceptorship Award for research excellence, NCR Award for teaching excellence, and Princeton University Graduate Mentoring Award. He has co-authored seven papers which have won the Best Paper Award at ICCD'93, FTCS'97, ICVLSID'98, DAC'99, PDCS'02, ICVLSID'03, and CODES'06. A paper of his was selected for "The Best of ICCAD: A collection of the best IEEE International Conference on Computer-Aided Design papers of the past 20 years," and another by IEEE Micro as being among the best of 2005 Computer Architecture conference papers. He has served as the Program Chairman of the 1992 Workshop on Fault-Tolerant Parallel and Distributed Systems and the 2004 International Conference on Embedded and Ubiquitous Computing where he gave the keynote speech on nanotechnology in 2005.

Vishwani D. Agrawal (F'86) received the B.E. degree from the University of Roorkee (renamed Indian Institute of Technology), Roorkee, India, in 1964, the M.E. degree from the Indian Institute of Science, Bangalore, India, in 1966, and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign, Urbana, in 1971.

He is the James J. Danaher Professor of Electrical and Computer Engineering at Auburn University, Auburn, AL. He has over 30 years of industry and university experience, working at Bell Laboratories, Murray Hill, NJ; Rutgers University, New Brunswick, NJ; TRW, Redondo Beach, CA; IIT, Delhi, India; EG&G, Albuquerque, NM; and ATI, Champaign, IL. His areas of work include VLSI testing, low-power design, and microwave antennas. He has published over 300 papers, has coauthored five books, and holds 13 U.S. patents. He is a co-author (along with M. L. Bushnell) of the textbook *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits* (Springer, 2000). He is the founder and Editor-in-Chief (1990–present) of the *Journal of Electronic Testing: Theory and Applications*, and a past Editor-in-Chief (1985–1987) of the *IEEE Design and Test of Computers Magazine*. Since 2003, he has served on the Editorial Board of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He is the Founder and Consulting Editor of the *Frontiers in Electronic Testing* Book Series of Springer. He is a co-founder of the *International Conference on VLSI Design*, and the *International Workshops on VLSI Design and Test*, held annually in India. He has served on numerous conference committees and is a frequently invited speaker. He was the invited Plenary Speaker at the 1998 International Test Conference, Washington D.C., and the Keynote Speaker at the Ninth Asian Test Symposium, Taiwan, R.O.C., in December 2000. During 1989 and 1990, he served on the Board of Governors of the IEEE Computer Society, and in 1994, chaired the Fellow Selection Committee of that Society.

Dr. Agrawal was a recipient of seven Best Paper Awards, two Honorable Mention Paper Awards, the Life-Time Achievement Award of the VLSI Society of India, in recognition of his contributions to the area of VLSI Test and for founding and steering the International Conference on VLSI Design in India, in 2006, the Harry H. Goode Memorial Award of the IEEE Computer Society, in 1998, for innovative contributions to the field of electronic testing, and the Distinguished Alumnus Award of the University of Illinois at Urbana-Champaign, in 1993, in recognition of his outstanding contributions in design and test of VLSI systems. He is a Fellow of the IETE-India (elected in 1983) and a Fellow of the ACM (elected in 2003). He has served on the advisory boards of the ECE Departments at University of Illinois, New Jersey Institute of Technology, and the City College of the City University of New York. (See his website *http://www.eng.auburn.edu\sim vagrawal*.)

Amine Bermak (M'99–SM'04) received the M.Eng. and Ph.D. degrees in electronic engineering from Paul Sabatier University, Toulouse, France, in 1994 and 1998, respectively.

He is currently an Assistant Professor with the Electronic and Computer Engineering Department, Hong Kong University of Science and Technology (HKUST), Clear Water Bay, Kowloon, Hong Kong, where he is also serving as the Associate Director of the Computer Engineering Program. During his Ph.D. studies, he was part of the Microsystems and Microstructures Research Group at the French National Research Center LAAS-CNRS, where he developed a 3-D VLSI chip for artificial neural network classification and detection applications. He then joined the Advanced Computer Architecture Research Group, York University, York, U.K., where he was working as a Post-doc on VLSI implementation of CMM neural network for vision applications in a project funded by British Aerospace. In 1998, he joined Edith Cowan University, Perth, Australia, first as a Research Fellow working on smart vision sensors, then as a Lecturer and a Senior Lecturer in the School of Engineering and Mathematics. His research interests include VLSI circuits and systems for signal, image processing, sensors, and microsystems applications. He has published extensively on these topics in various journals, book chapters, and refereed international conferences.

Dr. Bermak was a recipient of many distinguished awards, including the 2004 IEEE Chester Sall Award, HKUST Bechtel Foundation Engineering Teaching Excellence Award, in 2004, and a Best Paper Award at the 2005 International Workshop on System-On-Chip for Real-Time Applications. He is a member of technical program committees of a number of international conferences including the IEEE Custom Integrated Circuit Conference (CICC'06, CICC'07), the IEEE Consumer Electronics Conference (CEC'07), and Design Automation and Test in Europe (DATE'07). He is the general co-chair of the 2008 IEEE International Workshop on electronic design test and applications. He is a member of the IEEE CAS committee on sensory systems.
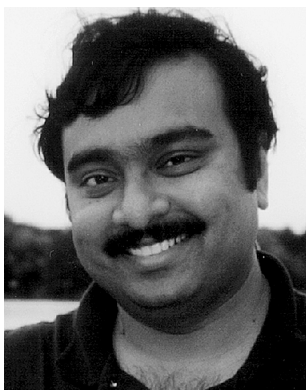
Chaitali Chakrabarti received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, and the M.S. and Ph.D. degrees in electrical engineering from the University of Maryland, College Park.

She has been a Professor at Arizona State University (ASU) since 1990. Her research interests include the areas of specialized architectures for signal processing and wireless communications, software defined radio, algorithm-architecture co-design, low power algorithms, and energy-efficient embedded system design including those powered by fuel cells.

Dr. Chakrabarti is a member of the Consortium of Embedded Systems and the Sensor, Signal, and Information Processing Center at ASU. She was a recipient of the Research Initiation Award from the National Science Foundation in 1993, a Best Teacher Award from the College of Engineering and Applied Sciences in 1994, and the Outstanding Educator Award from the IEEE Phoenix section in 2001. She has been on the program committees of ICASSP, ISCAS, SiPS, ASAP, DAC, and ISLPED. She served as an Associate Editor (AE) of the IEEE TRANSACTIONS ON SIGNAL PROCESSING (1999–2005) and also as an AE of the *Journal of VLSI Signal Processing Systems*. She is the Chair of the Technical Committee of Design and Implementation of Signal Processing Systems, IEEE Signal Processing Society.

Krishnendu Chakrabarty (SM'00) received the B.Tech. degree from the Indian Institute of Technology, Kharagpur, India, in 1990, and the M.S.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, in 1992 and 1995, respectively, all in computer science and engineering.

He is currently a Professor of Electrical and Computer Engineering at Duke University, Durham, NC. His current research projects include testing and design-for-testability of system-on-chip integrated circuits, microfluidic biochips, microfluidics-based chip cooling, and wireless sensor networks. He is the author of four books: *Microelectrofluidic Systems: Modeling and Simulation* (CRC, 2002), *Test Resource Partitioning for System-on-a-Chip* (Kluwer, 2002), *Scalable Infrastructure for Distributed Sensor Networks* (Springer, 2005), and *Digital Microfluidics Biochips: Synthesis, Testing, and Reconfigutaion Techniques* (CRC, 2006), and is the editor of the book volumes *SOC (System-on-a-Chip) Testing for Plug and Play Test Automation* (Kluwer, 2002) and *Design Automation Methods and Tools for Microfluidics-Based Biochips* (Springer, 2006). He is also an author of the forthcoming book *Adaptive Cooling of Integrated Circuits using Digital Microfluidics* (Artech House, April 2007). He has contributed over a dozen invited chapters to book volumes and published over 240 papers in archival journals and refereed conference proceedings. He holds a U.S. patent in built-in self-test and is a co-inventor of a pending U.S. patent on sensor networks.

Dr. Chakrabarty was a recipient of the National Science Foundation Early Faculty (CAREER) Award, the Office of Naval Research Young Investigator Award, Best Paper Awards at the 2007 IEEE International Conference on VLSI Design, the 2005 IEEE International Conference on Computer Design, the 2001 IEEE Design, Automation and Test in Europe (DATE) Conference, the Humboldt Research Fellowship, awarded by the Alexander von Humboldt Foundation, Germany, and the Mercator Visiting Professorship, awarded by the Deutsche Forschungsgemeinschaft, Germany. He is a Distinguished Visitor of the IEEE Computer Society for 2006–2007 and a Distinguished Lecturer of the IEEE Circuits and Systems Society for 2006–2007. He is an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, REGULAR PAPERS, the *ACM Journal on Emerging Technologies in Computing Systems*, an Editor of the IEEE DESIGN AND TEST OF COMPUTERS, and an Editor of *Journal of Electronic Testing: Theory and Applications (JETTA)*. He is a member of the editorial board for the *Microelectronics Journal*, *Sensor Letters*, and the *Journal of Embedded Computing*, and he serves as a subject area editor for the *International Journal of Distributed Sensor Networks*. In the recent past, he has also served as an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING. He is a senior member of ACM and a member of Sigma Xi. He served as the chair of the emerging technologies subcommittee for the IEEE International Conference on Computer-Aided Design (CAD) (2005–2006), and chairs the subcommittee for new, emerging, and specialized technologies for the 2006–2007 IEEE/ACM Design Automation Conference. He served as Tutorials Chair for the 2005 IEEE International Conference on VLSI Design and Program Chair for the 2005 IEEE Asian Test Symposium. He is the designated Program Chair for the CAD, Design, and Test Conference for the 2007 IEEE Symposium on Design, Integration, Test, and Packaging of MEMS/MOEMS (DTIP'07).

Kwang-Ting (Tim) Cheng (F'00) received the B.S. degree in electrical engineering from National Taiwan University, Taipei City, Taiwan, R.O.C., in 1983, and the Ph.D. degree in electrical engineering and computer science from the University of California, Berkeley, in 1988.

He worked at Bell Laboratories, Murray Hill, NJ, from 1988 to 1993, and joined the faculty at the University of California, Santa Barbara (UCSB), in 1993, where he is currently a Professor and Chair of the Electrical and Computer Engineering Department. He was the founding director of UCSB's Computer Engineering Program. His current research interests include design verification, test, silicon debug, and multimedia computing. He has published over 280 technical papers, co-authored three books, and holds ten U.S. Patents in these areas. He has also been working closely with U.S. industry and government agencies for projects in these areas.

Dr. Cheng was a recipient of Best Paper Awards at the 1994 Design Automation Conference and 1999 Design Automation Conference, a 2001 Annual Best Paper Award in the *Journal of Information Science and Engineering*, a Best Paper Award in 2003 at the Conference of Design Automation and Test in Europe (DATE 2003), and a Best Paper Award at the 1987 AT&T Conference on Electronic Testing. He currently serves as Editor-in-Chief for the IEEE DESIGN AND TEST OF COMPUTERS, an Associate Editor for the *ACM Transactions on Design Automation of Electronic Systems* and the *Formal Methods in System Design*, an Editor for the *Journal of Electronic Testing: Theory and Applications*, and an Editor for *Foundations and Trends in Electronic Design Automation*. He has served as General Chair and Program Chair of IEEE International Test Synthesis Workshop, Program Co-Chair of International Mixed-Signal Test Workshop, and served on the technical program committees for a number of international conferences on design, design automation, and test.

Robert Dick (S'95–M'02) received the Ph.D. degree from Princeton University, Princeton, NJ, and the B.S. degree from Clarkson University, Potsdam, NY.

He is an Assistant Professor at the Electrical Engineering and Computer Science Department, Northwestern University, Evanston, IL. He worked as a Visiting Professor in the Department of Electronic Engineering, Tsinghua University, Beijing, China, and a Visiting Researcher at NEC Laboratories America. He has published in the areas of embedded system synthesis, embedded operating systems, low-power and temperature-aware integrated circuit design, data compression, reliability, behavioral synthesis, and mobile ad-hoc network protocols.

Dr. Dick is a recipient of a National Science Foundation CAREER Award and the Best Teacher of the Year Award in 2004, from the Electrical Engineering and Computer Science Department. He serves on the technical program committees of several IEEE and ACM conferences.
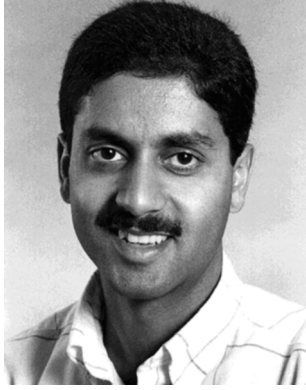
Nikil D. Dutt (SM'96) received the Ph.D. degree in computer science from the University of Illinois at Urbana-Champaign, Urbana, in 1989.

He is currently a Chancellor's Professor at the University of California, Irvine, with academic appointments in the Computer Science and Electrical Engineering and Computer Science Departments. His research interests include embedded systems design automation, computer architecture, optimizing compilers, system specification techniques, and distributed embedded systems.

Dr. Dutt is a recipient of Best Paper Awards at CHDL89, CHDL91, VLSIDesign 2003, CODES+ISSS 2003, CNCC 2006, and ASPDAC-2006. He was an ACM SIGDA Distinguished Lecturer during 2001-2002, and an IEEE Computer Society Distinguished Visitor for 2003-2005. He has served on the steering, organizing, and program committees of several premier computer-aided design (CAD) and embedded system design conferences and workshops, including ASPDAC, CASES, CODES+ISSS, DATE, ICCAD, ISLPED, LCTES, RTAS, and RTSS. He serves or has served on the advisory boards of ACM SIGBED and ACM SIGDA, and is Vice-Chair of IFIP WG 10.5.

Catherine H. Gebotys received the B.A.Sc. degree in engineering science and the M.A.Sc. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from the University of Waterloo, Waterloo, ON, Canada, in 1991.

She has been an Associate Professor with the Department of Electrical and Computer Engineering, University of Waterloo, since September 1991. She worked at Litton Systems Canada Ltd., Display Systems Engineering, from January 1985 to December 1986 in the area of computer-aided design (CAD) for VLSI and chip design. From January 1987 to August 1989, she was a Research Associate in the VLSI Group, Department of Electrical Engineering, University of Waterloo. She has published a number of research papers in the area of embedded security, side channel analysis and countermeasures, DSP processor power modeling and compilation, and optimization for high-level architectural synthesis. Her current research interests include security for portable devices, side channel analysis, and power/EM analysis countermeasures. Her research is funded in part by grants from Industry (RIM, Motorola, Alcatel) as well as NSERC, and OCE/CITO. She is the coauthor of the book *Optimal VLSI Architectural Synthesis: Area, Performance and Testability* (Kluwer, 1992).

Dr. Gebotys is a recipient of the CITO Champions of Innovation Award as well as a Best Paper Award. She is an Associate Editor for several journals (*Springer Journal on Design Automation for Embedded Systems (DAES)* and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATED (VLSI) SYSTEMS).

Joerg Henkel received the M.S. and Ph.D. (*summa cum laude*) degrees from the Technical University of Braunschweig, Braunschweig, Germany.

After graduation, he joined the Computer and Communication Research Laboratories (CCRL) (now NEC Laboratories America), Princeton, NJ, where he led various projects in the areas of low power system level design and advanced embedded architectures. In between, he had an appointment as a visiting professor at the University of Notre Dame, IN. He is currently with Karlsruhe University (TH), Karlsruhe, Germany, where he is a Director of the Chair for Embedded Systems (CES). He holds seven U.S. patents.

Dr. Henkel has served or is serving as a program committee member for major conferences in electronic design automation and embedded system design like DAC, ICCAD, DATE, ASP-DAC, CASES, Codes+ISSS, ECRTS, ISLPED, ISVLSI, RTSS, RSP, SCOPES, etc. He has given full-day tutorials at conferences like DAC, ICCAD, DATE, and others in the area of embedded system design. In 2001, he served as a Program Chair for the IEEE/ACM Codes Hardware/Software Co-Design Symposium and was a General Chair of the same convention in 2002. Furthermore, he was a Program Chair for the 2002 IEEE Workshop on Rapid System Prototyping. In 2006, he served as a Program Chair for the IEEE/ACM Symposium on Low Power Electronics and Design (ISLPED). He has guest-edited special issues on hardware/software co-design in the *IEEE Computer Magazine* and on rapid system prototyping with Kluwer. He is the Chair of the IEEE Computer Society, Germany Chapter.

Yehea Ismail was born in Giza, Egypt, on November 16, 1971. He received the B.Sc. degree in electronics and communications engineering (with distinction and honors), the M.S. degree in electronics (with distinction) from Cairo University, Cairo, Egypt, in 1993 and 1996, respectively, and the M.S. degree in electrical engineering and the Ph.D. degree from the University of Rochester, Rochester, NY, in 1998 and 2000, respectively.

He is currently an Associate Professor with Northwestern University, Evanston, IL. As one of the top of his class, he was appointed as a Teacher's Assistant in the Department of Electrical and Computer Engineering, Cairo University, in August of 1993. He was with IBM Microelectronics from 1997 to 1999. He is a co-author of more than 100 technical papers, a book, and several book chapters. His primary research interests include interconnect, noise, innovative circuit simulation, and related circuit level issues in high performance VLSI circuits.

Dr. Ismail is the chair elect of the CAS VLSI Technical Committee, on the editorial board of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, was on the editorial board of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, REGULAR PAPERS, and a guest editor for a special issue of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS on "On-Chip Inductance in High Speed Integrated Circuits." He has also chaired several conferences. He was a recipient of the 2002 IEEE circuits and systems society Outstanding Young Author Award, the National Science Foundation Career Award in 2002, and the Best Teacher Award in the Electrical Computer Engineering Department, Northwestern University, in 2003.

Ahmed Amine Jerraya received the Eng. degree from the University of Tunis, Tunis, Tunisia, in 1980, and the "Docteur Ingénieur" and the "Docteur d'Etat" degrees from the University of Grenoble, Grenoble, France, in 1983 and 1989, respectively, all in computer sciences.

Since February 2007, he has been with the Commissariat à l'énergie atomique/Laboratoire d'Électronique et de Technologie de l'Information (CEA/LETI), where he is acting as the Head of Design Programs for the advanced Design and System Division (DCIS). In 1986, he held a full research position with the Centre National de la Recherche Scientifique (CNRS). From April 1990 to March 1991, he was a Member of the Scientific Staff at Nortel, Canada, working on linking system design tools and hardware design environments. He received the grade of Research Director within CNRS and managed research dealing with Multiprocessor System-on-Chips at TIMA Laboratory. He co-authored eight books and published more than 200 papers in International Conferences and Journals.

Dr. Jerraya was a recipient of a Best Paper Award at the 1994 ED&TC for his work on hardware/software co-simulation. He served as General Chair for the Conference DATE in 2001.

Jing-Yang Jou (F'05) received the B.S. degree in electrical engineering from National Taiwan University, Taipei City, Taiwan, R.O.C., and the M.S. and Ph.D. degrees in computer science from the University of Illinois at Urbana-Champaign, Urbana, in 1979, 1983, and 1985, respectively.

He is currently the Director General of the National Chip Implementation Center, National Applied Research Laboratories, Taiwan, R.O.C. He is a Full Professor and was Chairman of the Electronics Engineering Department from 2000 to 2003 at National Chiao Tung University, Hsinchu, Taiwan, R.O.C. Before joining Chiao Tung University, he was with GTE Laboratories from 1995 to 1996 and with AT&T Bell Laboratories, Murray Hill, NJ, from 1986 to 1994. His research interests include logic and physical synthesis, design verification, CAD for low power and Network on Chips. He has published more than 160 technical papers.

Dr. Jou was a recipient of a Distinguished Paper Award of the IEEE International Conference on Computer-Aided Design in 1990, the Outstanding Academy-Industry Cooperation Achievement Award granted by the Ministry of Education (MOE), Taiwan, in 2002, and the Outstanding Electrical Engineering Professor Award from CIEE in 2006. He was elected President of the Taiwan Integrated Circuit Design Society (TICD) 2007–2008. He was the Technical Program Chair of the Asia-Pacific Conference on Hardware Description Languages (APCHDL'97), the Technical Program Chair of the 12th VLSI Design/CAD Symposium (2001), the Executive Chair of the 2nd Taiwan-Japan Microelectronics International Symposium (2002), the Honorary Chair of International Workshop on Multi-Project Chip (IWMC'06, 2006), and the Program Chair of the 2007 VLSI-DAT.

Srinivas Katkoori (SM'03) received the doctoral degree in computer engineering from the University of Cincinnati, Cincinnati, OH, in 1998.

In the Fall of 1997, he joined the Department of Computer Science and Engineering, University of South Florida, Tampa, as an Assistant Professor. In 2004, he was tenured and promoted to an Associate Professor. His research interests include the general area of VLSI computer-aided design (CAD) algorithms and design methodologies. His specific research areas include high level synthesis, low power synthesis, field-programmable gate array (FPGA) synthesis, and radiation tolerant CAD for FPGAs. To date, he has published over 50 peer-reviewed journal and conference papers. He holds one U.S. patent (6 963 217).

Dr. Katkoori was a recipient of the 2001 National Science Foundation (NSF) CAREER Award, the inaugural 2002–2003 University of South Florida Outstanding Faculty Research Achievement Award, and the 2005 Outstanding Engineering Educator Award from the IEEE Florida Council (Region 3). Besides NSF, his research sponsors include Honeywell, NASA JPL, and Florida I4 High Tech Corridor Initiative. He serves on the technical committees of several VLSI conferences and as a peer reviewer for several VLSI journals. He is a member of the ACM.

Sandip Kundu (F'07) is a Professor of Electrical and Computer Engineering at the University of Massachusetts, Amherst. Previously, he was a Principal Engineer at Intel Corporation and a Research Staff Member at IBM Corporation. He has published more than 75 papers in diverse areas including VLSI design, testing, computer-aided design (CAD), and coding and information theory. He holds 11 U.S. patents, has given more than a dozen tutorials at conferences.

Dr. Kundu served as an Associate Editor of the IEEE TRANSACTIONS ON COMPUTERS. He was the Technical Program Chair of ICCD in 2000 and the General Chair in 2001. He also served as a Co-General Chair of the VLSI 2005 conference. He is a distinguished visitor of IEEE Computer Society.

Volkan Kursun (S'01–M'04) received the B.S. degree in electrical and electronics engineering from the Middle East Technical University, Ankara, Turkey, in 1999, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Rochester, Rochester, NY, in 2001 and 2004, respectively.

He joined the Department of Electrical and Computer Engineering, University of Wisconsin-Madison, Madison, as an Assistant Professor in 2004. He performed research on mixed-signal thermal inkjet integrated circuits with Xerox Corporation, Webster, NY, in 2000. During the summers of 2001 and 2002, he was with Intel Microprocessor Research Laboratories, Hillsboro, OR, where he was responsible for the modeling and design of high frequency monolithic power supplies. His current research interests include the areas of low voltage, low power, and high performance integrated circuit design, modeling of semiconductor devices, and emerging integrated circuit technologies. He has more than fifty publications and two issued and five pending U.S. patents in the areas of high performance integrated circuits and emerging semiconductor technologies. He is the author of the book *Multi-Voltage CMOS Circuit Design* (Wiley, 2006).

He is a member of the technical program and organizing committees of a number of IEEE and ACM conferences and serves on the editorial boards of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: BRIEF PAPERS and the *Journal of Circuits, Systems, and Computers*.

Sung Kyu Lim received the B.S., M.S., and Ph.D. degrees in computer science from the University of California, Los Angeles (UCLA), in 1994, 1997, and 2000, respectively.

From 2000 to 2001, he was a Post-Doctoral Scholar at UCLA, and a Senior Engineer at Aplus Design Technologies, Inc. He joined the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, in 2001, where he is currently an Associate Professor. His research focus is on the physical design automation for 3-D circuits, 3-D system-on-packages, microarchitectural physical planning, and field-programmable analog arrays.

Dr. Lim is a recipient of the Design Automation Conference (DAC) Graduate Scholarship in 2003 and the National Science Foundation Faculty Early Career Development (CAREER) Award in 2006. He has been on the Advisory Board of the ACM Special Interest Group on Design Automation (SIGDA) since 2003. He is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and served as a Guest Editor for the *ACM Transactions on Design Automation of Electronic Systems* (TODAES). He has served on the Technical Program Committee of several ACM and IEEE conferences on electronic design automation.

Sharad Malik (F'02) received the B. Tech. degree in electrical engineering from the Indian Institute of Technology, New Delhi, India, in 1985, and the M.S. and Ph.D. degrees in computer science from the University of California, Berkeley, in 1987 and 1990, respectively.

Currently, he is the George Van Ness Lothrop Professor of Engineering and the Director for the Center for Innovation in Engineering Education at Princeton University, Princeton, NJ. His research interests span all aspects of electronic design automation. His current focus areas are the synthesis and verification of digital systems and embedded computer systems. He has published numerous papers, book chapters, and a book (*Static Timing Analysis for Embedded Software*) describing his research. His research in functional timing analysis and propositional satisfiability has been widely used in industrial electronic design automation tools.

Dr. Malik was a recipient of the Princeton University School of Engineering and Applied Sciences Distinguished Teacher Award (2005), the Princeton University Engineering Council Excellence in Teaching Award (1995, 1994, and 1993), the Walter C. Johnson Prize for Teaching Excellence (1993), Best Paper Awards at the IEEE/ACM Design Automation and Test in Europe Conference (2003), ACM/IEEE Design Automation Conference (1996), and the IEEE International Conference on Computer Design (1992), the National Science Foundation's (NSF's) Young Investigator Award (1994), Princeton University Rheinstein Faculty Award (1994), the IBM Faculty Development Award (1991), an NSF Research Initiation Award (1992), and the President of India's Gold Medal for academic excellence (1985). He serves/has served on the program committees of the Design Automation Conference (DAC), International Conference on Computer-Aided Design, and International Conference on Computer Design, and as the General Chair for DAC 2004. He serves as Associate Editor for the *ACM Transactions on Design Automation of Electronic Systems*, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and Editor-in-Chief for NOW Publishers' Foundations and Trends in Electronic Design Automation. He is also on the editorial boards of the *Journal of VLSI Signal Processing*, *Design Automation for Embedded Systems*, and the IEEE DESIGN AND TEST. He is currently serving as the Associate Director of the MARCO/DARPA Gigascale Systems Research Center, a multi-university effort directed towards defining and developing electronic system design methodology with a ten year horizon.

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He is an Associate Professor of Electrical and Computer Engineering at Cornell University, Ithaca, NY, where his group conducts research on asynchronous design. He has also been a member of the Cornell faculty since 1998, where he co-founded its Computer Systems Laboratory. He was one of the principal designers of MiniMIPS, the first high-performance asynchronous microprocessor. His group has developed several asynchronous VLSI systems, including the first microprocessor for sensor networks, an event-based chip-multiprocessor, and a pipelined field-programmable gate array (FPGA).

Dr. Manohar was a recipient of a National Science Foundation (NSF) CAREER Award, two Best Paper Awards, five Teaching Awards, and was named to MIT technology review's top 35 young innovators under the age of 35 (2005).

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Dr. Marculescu was a recipient of a National Science Foundation Faculty Career Award (2000–2004), an ACM-SIGDA Technical Leadership Award (2003), the Carnegie Institute of Technology George Tallman Ladd Research Award (2004), and a Best Paper Award from IEEE Asia South-Pacific Design Automation Conference (ASPDAC 2005). She was an IEEE-Circuits and Systems Society Distinguished Lecturer (2004–2005) and is currently the Chair of the ACM Special Interest Group on Design Automation (SIGDA).

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Dr. Massoud was a recipient of the Synopsys Special Recognition Engineering Award, a Best Paper Award at the International Symposium on Quality Electronic Design, ISQED, in 2007, and the National Science Foundation CAREER Award for 2004.

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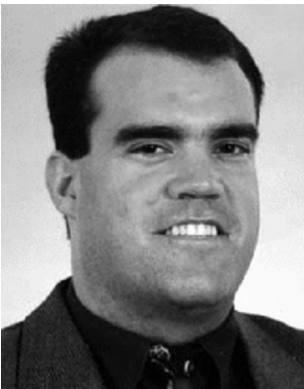
Vincent J. Mooney III (S'94–M'98–SM'04) received the B.S. degree from Yale University, New Haven, CT, in 1991, where he double majored in electrical engineering and computer science, and the M.S. degree in electrical engineering, M.A. degree in philosophy, and Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1994, 1997, and 1998, respectively.

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Prof. Peng was a recipient of two Best Paper Awards at the European Design Automation Conferences (1992 and 1994), a Best Paper Award at the IEEE Asian Test Symposium (2002), a Best Paper Award at the Design Automation and Test in Europe Conference (2005), and a Best Presentation Award at the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (2003). He serves as an Associate Editor of the *VLSI Design Journal* and the *EURASIP Journal on Embedded Systems*. He has served as the Guest Editor for the special issue on "Emerging Strategies for Resource-Constrained Testing of System Chips" in the *IEE Proceedings for Computer and Digital Techniques* and the special issue on "Design Methodologies and Tools for Real-Time Embedded Systems" in the *Journal on Design Automation for Embedded Systems*. He has served on the program committee of a dozen international conferences and workshops, including ATS, ASP-DAC, DATE, DDECS, DFT, ETS, ITSW, MEMOCDE, and VLSI-SOC. He was the General Chair of the 6th IEEE European Test Workshop (ETW 01), the Program Chair of the 7th IEEE Design and Diagnostics of Electronic Circuits and Systems Workshop (DDECS 04), and the Test Track Chair of the 2006 Design Automation and Test in Europe Conference (DATE 06). He is the Program Chair of the 12th IEEE European Test Symposium (ETS 07), and the Vice Program Chair of DATE 07. He is currently the Chair of the IEEE European Test Technology Technical Council (ETTTC), and has been a Golden Core Member of the IEEE Computer Society since 2005.

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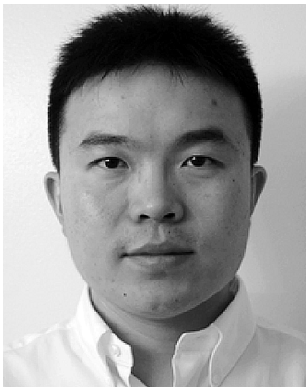
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Dr. Shang's work on thermal-aware on-chip network was selected for publication in MICRO Top Pick 2006. He was also a recipient of the Best Paper Award at PDCS'02 and the Department of Electrical and Computer Engineering's Teaching Award in 2006. He is the Walter F. Light Scholar of Queen's University.

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Dr. Sur-Kolay was a recipient of the President of India Gold Medal (*summa cum laude)* at IIT Kharagpur in 1980. She has served on the Program Committees of many International Conferences and was the Technical Program Chair of the 18th International Conference on VLSI Design, 2005. She has also been reviewer for many international journals and is presently on the editorial board of *Proceedings of IEE CDT*. She is a member of IEE and VLSI Society of India.

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