Editorial Appointments for the 2009-2010 Term

IT IS with great pleasure that I introduce the new editorial board for the new 2009–2010 term. To address the increase in the number of TVLSI submissions, the size of the editorial board has now been increased by more than a third relative to the last term. First, I thank and commend the Associate Editors (AEs) on the previous editorial board for selflessly committing their time to ensure timely reviews and decisions. Indeed, their tireless efforts brought down the average decision time to just 77 days. Some of the previous AEs will continue. However, around half the AEs in the new editorial board are new. They not only bring fresh energy to TVLSI, but also cover significantly more diverse areas, so that we are able to serve the TVLSI community better and bring down the average decision time further. Even the AEs who are not serving on the new editorial board will continue to bring the review process of previous papers assigned to them to completion. This will provide seamless continuity from the previous editorial board to the next.

I would like to thank the TVLSI Steering Committee and its Chairman, Prof. Eby Friedman, for agreeing to allow 200 extra pages for TVLSI. This will help us reduce the publication backlog. I also thank them for their periodic advice.

I am also thankful to Prof. Yehea Ismail for agreeing to continue as the Associate Editor-in-Chief. I value the counsel he has provided in the last term and look forward to taking advantage of his expertise and wisdom in the coming term.

I would also like to thank Ms. Mona Mittra, Ms. Michelle Nixon, Ms. Sonal Parikh, Mr. Richard Jannuzzi, and other staff members for all their efforts to keep TVLSI running smoothly. Last, but not the least, I want to express my deep gratitude to the TVLSI Editorial Assistant, Ms. Stacey Weber Jackson, for her steady and extremely efficient service to TVLSI.

The biographies and photographs of the AEs on the new editorial board are provided as follows.

NIRAJ K. JHA
Department of Electrical Engineering
Princeton University
Princeton, NJ 08544 USA

Digital Object Identifier 10.1109/TVLSI.2009.2014706

Niraj K. Jha (S'85–M'85–SM'93–F'98) received the B.Tech. degree in electronics and electrical communication engineering from Indian Institute of Technology, Kharagpur, India, in 1981, the M.S. degree in electrical engineering from S.U.N.Y., Stony Brook, NY, in 1982, and the Ph.D. degree in electrical engineering from University of Illinois, Urbana, IL, in 1985.

He is a Professor with the Department of Electrical Engineering, Princeton University, Princeton, NJ. He has coauthored three books titled *Testing and Reliable Design of CMOS Circuits* (Kluwer, 1990), *High-Level Power Analysis and Optimization* (Kluwer, 1998), and *Testing of Digital Systems* (Cambridge University Press, 2003). He has also authored ten book chapters. He has authored or coauthored more than 330 technical papers. He holds 13 U.S. patents. His research interests include nanotechnology, low power hardware/software design, computer-aided design of integrated circuits and systems, digital system testing and secure computing.

Dr. Jha was a recipient of the AT&T Foundation Award and NEC Preceptorship Award for research excellence, NCR Award for teaching excellence, and Princeton University Graduate Mentoring Award. He has coauthored seven papers which have won the Best Paper Award at ICCD'93, FTCS'97, ICVLSID'98, DAC'99, PDCS'02, ICVLSID'03, and CODES'06. A paper of his was selected for ''The Best of ICCAD: A collection of the best IEEE International Conference on Computer-Aided Design papers of the past 20 years,'' two papers by IEEE Micro Magazine as one of the top picks from the 2005 and 2007 Computer Architecture conferences, and two others as being among the most influential papers of the last 10 years at IEEE Design Automation and Test in Europe Conference. He is currently serving as the Editor-in-Chief of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, and the *Journal of Low Power Electronics*. He has served as an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS and the *Journal of Electronic Testing: Theory and Applications* in the past. He has also served as the Program Chairman of the 1992 Workshop on Fault-Tolerant Parallel and Distributed Systems and the 2004 International Conference on Embedded and Ubiquitous Computing. He has served as the Director of the Center for Embedded System-on-a-Chip Design funded by New Jersey Commission on Science and Technology. He is a Fellow of the ACM.

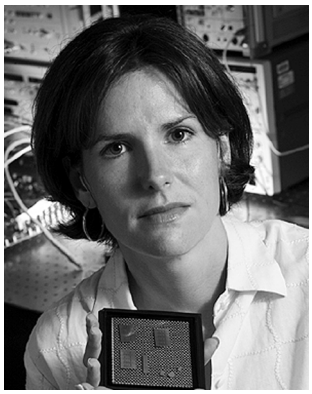
1063-8210/$25.00 © 2009 IEEE

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.

Massimo Alioto (M'01–SM'07) was born in Brescia, Italy, in 1972. He received the laurea degree in electronics engineering and the Ph.D. degree in electrical engineering from the University of Catania, Catania, Italy, in 1997 and 2001, respectively.

In 2002, he joined the Dipartimento di Ingegneria dell'Informazione (DII), the University of Siena, Arezzo, Italy, as a Research Associate and in the same year as an Assistant Professor. In 2005, he was appointed an Associate Professor of Electronics, and was engaged in the same faculty in 2006. In the summer of 2007, he was a Visiting Professor at EPFL, Lausanne, Switzerland. In 2009-2010, he spends a year as a Visiting Professor with BWRC, University of California, Berkeley. He is the director of the Electronics Lab, University of Siena. Since 2001, he has been teaching undergraduate and graduate courses on advanced VLSI digital design, microelectronics, and basic electronics. He has authored or coauthored about 120 publications on journals (over 40, mostly IEEE Transactions) and conference proceedings. Two of them are among the 25 most downloaded TVLSI papers in 2007 (respectively 10th and 13th). He is coauthor of the book Model and Design of Bipolar and MOS Current-Mode Logic: CML, ECL, and SCL Digital Circuits (Springer, 2005). His primary research interests include the modeling and the optimized design of CMOS high-performance, low-power, and ultra low-power digital circuits, arithmetic, and cryptographic circuits, interconnect modeling, design/modeling for variability-tolerant and low-leakage VLSI circuits, circuit techniques for emerging technologies.

Prof. Alioto is a member of the HiPEAC Network of Excellence. He is the Chair Elect of the "VLSI Systems and Applications" Technical Committee of the IEEE Circuits and Systems Society, for which he is also Distinguished Lecturer. He is regularly invited to give talks to academic institutions and conferences throughout the world. He has served as a member of various conference technical program committees (ISCAS, PATMOS, ICM, ICCD, CSIE) and Track Chair (ICECS, ISCAS). He serves as Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, as well as of *Integration—The VLSI Journal* (Elsevier), *Journal of Circuits, Systems, and Computers*, and also of *Microelectronics Journal* (Elsevier). He is Guest Editor of the Special Issue "High speed random bit generators" of the International Journal of High Speed Electronics and Systems (2008).



Alyssa Apsel (M'99) received the B.S. degree from Swarthmore College, Swarthmore, PA, in 1995, the M.S. degree in electrical engineering from California Institute of Technology, Pasadena, in 1996, and the Ph.D. degree in electrical engineering from Johns Hopkins University, Baltimore, MD, in 2002, respectively.

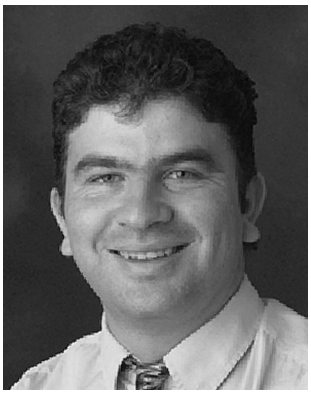
She joined the Department of Electrical and Computer Engineering, Cornell University, Ithaca, NY, in 2002, where she is currently an Associate Professor. The focus of her research is on mixed signal circuits and solving the problems that arise in highly scaled CMOS and modern electronic systems. She has coauthored over 65 refereed publications in the fields of optical interconnect design and planning, photonic integration with VLSI, circuit design techniques in the presence of variation, and mixed signal circuit design, resulting in four patents and several pending patent applications.

Dr. Apsel was a recipient of a Best Paper Award from ASYNC 2006, a MICRO "Top Picks" paper in 2006, a College Teaching Award in 2007, the National Science Foundation CAREER Award in 2004, and was selected by Technology Review Magazine as one of the Top 100 Young Innovators in 2004. She also serves on technical committees for ISCAS, has served as a member of the Science and Engineering Council of the OSA, and as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: BRIEF PAPERS.

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.

Iris Bahar received the B.S. and M.S. degrees in computer engineering from the University of Illinois, Urbana-Champaign, and the Ph.D. degree in electrical and computer engineering from the University of Colorado, Boulder.

Since 1996, she has been with the Division of Engineering, Brown University, Providence, RI, where she is currently an Associate Professor. From 1987 to 1992, she worked for Digital Equipment Corporation (in what is now the Intel Hudson facility), and was part of the NVAX microprocessor design team. Her research interests include power-aware computer architecture; computer-aided design for synthesis, verification, and low-power applications; and design, test, and reliability issues for nanoscale systems.



Amine Bermak (M'99–SM'04) received the M.Eng. and Ph.D. degrees in electronic engineering from Paul Sabatier University, Toulouse, France, in 1994 and 1998, respectively.

During his Ph.D., he was part of the Microsystems and Microstructures Research Group, French National Research Center LAAS-CNRS, where he developed a 3-D VLSI chip for artificial neural network classification and detection applications. He then joined the Advanced Computer Architecture Research Group, York University, York, England, where he was working as a Post-doc on VLSI implementation of CMM neural network for vision applications in a project funded by British Aerospace. In 1998, he joined Edith Cowan University, Perth, Australia, first as a research fellow working on smart vision sensors, then as a Lecturer and a Senior Lecturer in the School of Engineering and Mathematics. He is currently an Associate Professor with the Electronic and Computer Engineering Department, Hong Kong University of Science and Technology (HKUST), where he is also serving as the director of Computer Engineering and the director of M.Sc. degree in Integrated Circuit Design (ICDE). His research interests are related to VLSI circuits and systems for signal, image processing, sensors, and microsystems applications. He has published extensively on the above topics in various journals, book chapters, and refereed international conferences.

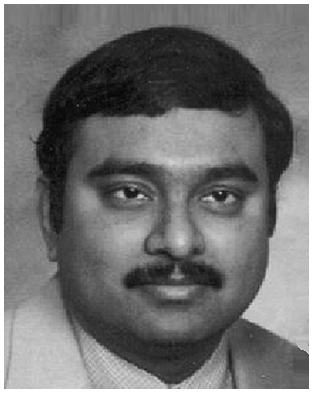
Dr. Bermak was a recipient of many distinguished awards, including the 2004 "IEEE Chester Sall Award", the HKUST "Bechtel Foundation Engineering Teaching Excellence Award" in 2004, and the "Best Paper Award" at the 2005 International Workshop on System-On-Chip for Real-Time Applications. He is a member of technical program committees of a number of international conferences including the IEEE Custom Integrated Circuit Conference CICC'2006, CICC'2007, the IEEE Consumer Electronics Conference CEC'2007, Design Automation, and Test in Europe DATE2007, DATE2008. He is the general cochair of the IEEE International Symposium on electronic design test and applications, Hong Kong 2008, and the general cochair of the IEEE Conference on Biomedical Circuits and Systems, Beijing, 2009. He is also on the Editorial Board of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and the *Journal of Sensors*. Dr Bermak is a member of IEEE CAS committee on sensory systems.

Chaitali Chakrabarti received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, and the M.S. and Ph.D. degrees in electrical engineering from the University of Maryland, College Park.

She has been a Professor with Arizona State University (ASU), Tempe, since 1990. Her research interests include the areas of specialized architectures for signal processing and wireless communications, software defined radio, algorithm-architecture codesign, low power algorithms, and energy-efficient embedded system design including those powered by fuel cells.

Dr. Chakrabarti was a recipient of the Research Initiation Award from the National Science Foundation in 1993, a Best Teacher Award from the College of Engineering and Applied Sciences in 1994, and the Outstanding Educator Award from the IEEE Phoenix section in 2001. She is a member of the Consortium of Embedded Systems and the Sensor, Signal, and Information Processing Center at ASU. She has been on the program committees of ICASSP, ISCAS, SiPS, ASAP, DAC, and ISLPED. She served as an Associate Editor (AE) of the IEEE TRANSACTIONS ON SIGNAL PROCESSING (1999–2005) and also as an AE of the *Journal of VLSI Signal Processing Systems*. She is the Chair of the Technical Committee of Design and Implementation of Signal Processing Systems, IEEE Signal Processing Society.

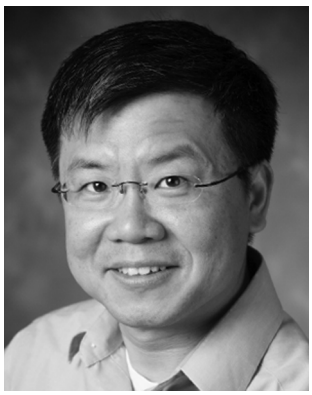
Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.



Krishnendu Chakrabarty (F'08) received the B.Tech. degree from the Indian Institute of Technology, Kharagpur, India, in 1990, and the M.S.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, in 1992 and 1995, respectively.

He is currently a Professor with the Department of Electrical and Computer Engineering, Duke University, Durham, NC. His current research projects include testing and design-for-testability of integrated circuits, digital microfluidics and biochips, circuits and systems based on DNA self-assembly, and wireless sensor networks. He has authored seven books on these topics, published 300 papers in journals and refereed conference proceedings, and given over 120 invited, keynote, and plenary talks.

Prof. Chakrabarty was a recipient of the National Science Foundation Early Faculty (CAREER) Award, the Office of Naval Research Young Investigator Award, the Humboldt Research Fellowship from the Alexander von Humboldt Foundation, Germany, and several Best Papers Awards at IEEE conferences, and the 2008 Duke University Graduate School Dean's Award for excellence in mentoring. He is a Distinguished Engineer of ACM. He is a 2009 Fellow of the Japan Society for the Promotion of Science (JSPS). He served as a Distinguished Visitor of the IEEE Computer Society during 2005–2007, and as a Distinguished Lecturer of the IEEE Circuits and Systems Society during 2006–2007. Currently he serves as an ACM Distinguished Speaker. He is an Associate Editor of IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and the *ACM Journal on Emerging Technologies in Computing Systems*. He also serves as an Editor of *IEEE Design & Test of Computers* and of the *Journal of Electronic Testing: Theory and Applications* (JETTA).



Deming Chen received the B.S. degree from University of Pittsburgh, Pittsburgh, PA, in 1995 and the Ph.D. degree from University of California at Los Angeles, Los Angeles, in 2005, all from the Computer Science Department.

He worked as a Software Engineer between 1995-1999 and 2001-2002. He joined the Electrical and Computer Engineering Department, UIUC as a faculty member in 2005. His current research interests include nano-systems design, CAD for FPGAs, microprocessor architecture design under process/parameter variation, and reconfigurable computing.

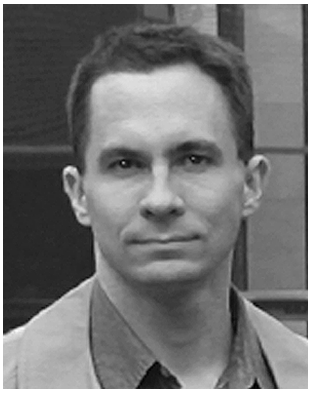
Dr. Chen was a recipient of the Achievement Award for Excellent Teamwork from Aplus Design Technologies in 2001, the Arnold O. Beckman Research Award from UIUC in 2007, the NSF CAREER Award in 2008, and the Best Paper Award from ASPDAC in 2009. He is a technical committee member and session chair for a series of conferences and symposiums. He is a subcommittee chair for ASPDAC and a CAD Track chair for ISVLSI. He was included in the List of Teachers Ranked as Excellent in 2008.

Kwang-Ting (Tim) Cheng (F'08) received the B.S. degree in electrical engineering from National Taiwan University, Taiwan, in 1983 and the Ph.D. degree in electrical engineering and computer science from the University of California, Berkeley, in 1988.

He worked with Bell Laboratories, Murray Hill, NJ, from 1988 to 1993 and joined the faculty at the University of California, Santa Barbara in 1993 where he is currently a Professor of the Electrical and Computer Engineering Department. He was the founding director of UCSB's Computer Engineering Program (1999-2002) and Chair of the ECE Department (2005-2008). His current research interests include design verification, test, silicon debug, and multimedia computing. He has published over 300 technical papers, coauthored four books, and holds 11 U.S. patents in these areas. He has also been working closely with US industry and government agencies for projects in these areas.

Dr. Cheng was a recipient of Best Paper Awards at the 1994 and 1999 Design Automation Conferences, 2003 Conference of Design Automation and Test in Europe (DATE 2003), 2007 Asian Test Symposium, 1987 AT&T Conference on Electronic Testing, 2001 Annual Best Paper Award in Journal of Information Science and Engineering and the UCSB College of Engineering's Outstanding Teaching Faculty Award for 2004–2005. He currently serves as Editor-in-Chief for *IEEE Design and Test of Computers*, Associate Editor for *ACM Transactions on Design Automation of Electronic Systems*, Associate Editor for *Formal Methods in System Design*, Editor for *Journal of Electronic Testing: Theory and Applications*, and Editor for *Foundations and Trends in Electronic Design Automation*. He had served as General Chair and Program Chair of IEEE International Test Synthesis Workshop, Program Co-Chair of International Mixed-Signal Test Workshop and served on the technical program committees for a number of international conferences on design, design automation, and test.

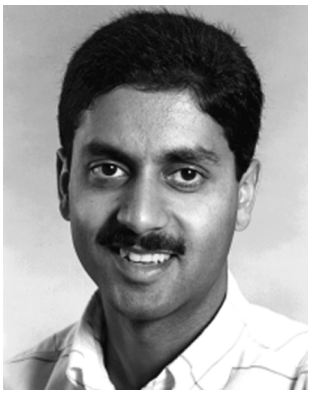
Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.



Robert Dick (S'95-M'02) received the B.S. degree from Clarkson University, Potsdam, NY, and the Ph.D. degree from Princeton University, Princeton, NJ.

He is an Associate Professor with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor. He worked as a Visiting Professor with the Department of Electronic Engineering, Tsinghua University, as a Visiting Researcher with NEC Labs America, and as an Associate Professor with Northwestern University. He has published in the areas of embedded operating systems, data compression, embedded system synthesis, dynamic power management, low-power and temperature-aware integrated circuit design, wireless sensor networks, human perception aware computer design, reliability, embedded system security, and behavioral synthesis.

Dr. Dick was a recipient of an NSF CAREER Award and won his department's Best Teacher of the Year Award in 2004. His technology won a Computerworld Horizon Award and his paper was selected by DATE as one of the 30 most influential in the past 10 years in 2007. He served as a technical program subcommittee chair for the International Conference on Hardware/Software Codesign and System Synthesis. He is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and serves on the technical program committees of several embedded systems and CAD/VLSI conferences.



Nikil D. Dutt (F'08) received the Ph.D. in computer science from the University of Illinois at Urbana-Champaign, Urbana-Champaign, in 1989.

He is currently a Chancellor's Professor with the University of California, Irvine, with academic appointments in the Computer Science and Electrical Engineering and Computer Science Departments. His research interests include embedded systems design automation, computer architecture, optimizing compilers, system specification techniques, and distributed embedded systems.

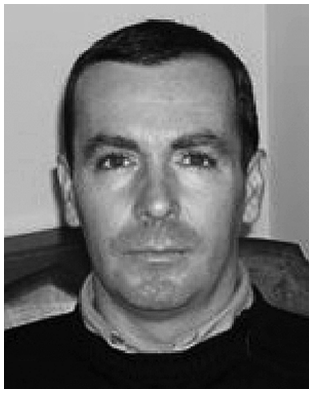
Dr. Dutt was a recipient of Best Paper Awards at CHDL89, CHDL91, VLSIDesign2003, CODES+ISSS 2003, CNCC 2006, and ASPDAC-2006. He was an ACM SIGDA Distinguished Lecturer during 2001–2002, and an IEEE Computer Society Distinguished Visitor for 2003–2005. He has served on the steering, organizing, and program committees of several premier CAD and Embedded System Design conferences and workshops, including ASPDAC, CASES, CODES+ISSS, DATE, ICCAD, ISLPED, LCTES, RTAS, and RTSS. He serves or has served on the advisory boards of ACM SIGBED and ACM SIGDA and is Vice-Chair of IFIP WG 10.5.

Catherine Gebotys received the B.A.Sc. degree in engineering science and the M.A.Sc. degree in electrical engineering from University of Toronto, Toronto, ON, Canada, in 1982 in 1984, respectively, and the Ph.D. degree in electrical engineering from the University of Waterloo, Waterloo, ON, Canada, in 1991.

She worked with Litton Systems Canada Ltd. from January 1985 to December 1986 in the area of CAD for VLSI and chip design. From January 1987 to August 1989, she was a Research Associate with the VLSI Group, Department of Electrical Engineering, University of Waterloo, where she is currently a Professor and has been with the Department of Electrical and Computer Engineering since September 1991. She is the inventor of several pending patents. Her research interests include embedded systems security, side channel (power/electromagnetic) analysis of cryptographic algorithms, reconfigurable computing models, global optimization approaches to compilation for DSP processors, low-power systems synthesis, and high-level architectural synthesis.

Dr. Gebotys was a recipient of the CITO Champions of Innovation Award, as well as a Best Paper Award. She was Technical Program Co-Chair of CODES+ISSS 2008 and she has served on several technical program committes (CODES+ISSS, International Symposium on System Synthesis, DATE). She is an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and an Associate Editor for *DAES the Springer Verlag Journal*.

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.



Patrick Girard received the M.S. degree in electrical engineering and the Ph.D. degree in microelectronics from the University of Montpellier, France, in 1988 and 1992, respectively.

He is currently a Research Director with CNRS (French National Center for Scientific Research), and works in the Microelectronics Department, LIRMM (Laboratory of Informatics, Robotics and Microelectronics), Montpellier, France. His research interests include the various aspects of digital testing and memory testing, with special emphasis on DfT, BIST, diagnosis, delay testing, and power-aware testing. He has supervised 20 Ph.D. dissertations and has published 6 books or book chapters, 30 journal papers, and more than 110 conference and symposium papers on these fields.

Dr. Girard was a recipient of the Best Paper Award at ETS 2004 and at DDECS 2005. He is the Vice-Chair of the European Test Technology Technical Council (ETTTC) of the IEEE Computer Society. He is currently the Editor-in-Chief of the *ASP Journal of Low Power Electronics* (JOLPE) and an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and the *Journal of Electronic Testing—Theory and Applications* (JETTA—Springer). From 2005 to 2009, he was an Associate Editor of the IEEE TRANSACTIONS ON COMPUTERS. He has served as technical program committee member of the ACM/IEEE Design Automation Conference (DAC), ACM/IEEE Design Automation and Test in Europe (DATE), IEEE International Test Conference (ITC), IEEE International Conference on Computer Design (ICCD), IEEE International Conference on Design & Test of Integrated Systems (DTIS), IFIP International Conference on VLSI-SOC, IEEE VLSI Test Symposium (VTS), IEEE European Test Symposium (ETS), IEEE International On-Line Testing Symposium (IOLTS), IEEE Asian Test Symposium (ATS), ACM/IEEE International Symposium on Low Power Electronic Design (ISLPED), IEEE International Symposium on Electronic Design, Test & Applications (DELTA) and IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS). He has served as Test Track Chair for DAC 2007, DATE 2007, DATE 2008, ICCD 2008, and DATE 2009. He has also served as Program Chair for DELTA 2006, DTIS 2006, DDECS 2007, and ETS 2008. He has been involved in several European research projects (ESPRIT III ATSEC, EUREKA MEDEA, MEDEA+ ASSOCIATE, IST MARLOW, MEDEA+ NanoTEST, CATRENE TOETS) and has managed industrial research contracts with major companies like Infineon Technologies, Atmel, STMicroelectronics, etc.

Dimitris Gizopoulos (SM'03) received the Engineering Diploma from the Computer Engineering and Informatics Department, University of Patras, Patras, Greece, in 1992, and the Ph.D. degree from the Department of Informatics and Telecommunications, University of Athens, Athens, Greece, in 1997, both with honors.

He is an Associate Professor with the Department of Informatics, University of Piraeus, Piraeus, Greece where he leads the Computer Systems Laboratory. His research interests include microprocessors, microprocessor-based systems and multiprocessors design, test and fault tolerance, general purpose and embedded computing systems dependable design including self-testing, online testing and fault tolerance solutions. He has published more than 90 papers in peer reviewed transactions, journals and conference proceedings, is coinventor of a U.S. patent, author of a book, and editor of a second in test technology, both published by Springer.

Dr. Gizopoulos is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, the IEEE TRANSACTIONS ON COMPUTERS, the *IEEE Design & Test of Computers Magazine*, as well as Springer's *Journal of Electronic Testing: Theory and Applications*, as well as Guest Editor for Special Issues in IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, *IEEE Design & Test of Computers Magazine*, and *IEEE Communications Magazine*. Since 2004, he is member of the Steering Committee of the IEEE International Test Conference (ITC) and between 2001 and 2006 member of the Steering Committee of the IEEE European Test Symposium (ETS). He was General Chair of the IEEE European Test Workshop 2002, the IEEE International On-Line Testing Symposium 2003, and is the General Chair of the IEEE International Symposium on Defect and Fault Tolerance 2009. He was Program Chair of the IEEE International On-Line Testing Symposium 2007 and 2008 and the IEEE International Symposium on Defect and Fault Tolerance 2008 and is the Program Chair of the IEEE International On-Line Testing Symposium 2009. He is also a member of the Organizing and Program Committees of several IEEE conferences. He is a member of the Executive Committee of the IEEE Computer Society Test Technology Technical Council (TTTC) with contributions as the Technical Meetings Group chairman and as Test Technology Educational Program chairman. He is a Golden Core Member of IEEE Computer Society.

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.

Jörg Henkel is currently with Karlsruhe University (TH), Karlsruhe, Germany, where he is directing the Chair for Embedded Systems CES. Before, he was with NEC Laboratories, Princeton, NJ. His current research is focused on design and architectures for embedded systems with focus on low power and reliability. He holds nine U.S. patents.

Dr. Henkel was a recipient of the 2008 DATE Best Paper Award. He has organized various embedded systems and low power ACM/IEEE conferences/symposia as General Chair and Program Chair and was a Guest Editor on these topics in various Journals like the *IEEE Computer Magazine*. Currently (2009), he is the General Chair of the IEEE/ACM Symposium on Low Power Electronics and Design ISLPED'09 and the General Chair of the IEEE/ACM CASES Conference. He is/has been a steering committee member of major conferences in the embedded systems field like at ICCAD, Codes+ISSS and is also an editorial board members of various journals like the IEEE TVLSI, JOLPE, etc. He has given full/half-day tutorials at leading conferences like DAC, ICCAD, DATE, etc. He is the Chairman of the IEEE Computer Society, Germany Section, and the Editor-in-Chief of the *ACM Transactions on Embedded Computing Systems* (ACM TECS).

Yehea Ismail was born in Giza, Egypt, on November 16, 1971. He received the B.Sc. degree in electronics and communications engineering with distinction and honors and the Masters degree in electronics (distinction) from the School of Engineering, Department of Electronics and Communications, Cairo University, Cairo, Egypt, in 1993 and 1996, respectively, and the M.S. and Ph.D. degrees from the University of Rochester, Rochester, NY, in 1998 and 2000, respectively, both in electrical engineering.

As one of the top of his class, he was appointed as a Teacher Assistant with the Department of Electrical and Computer Engineering, Cairo University, in August 1993. He is currently a Professor with Northwestern University, Evanston, IL, and at Nile University, El Sheikh Zayed City, Egypt, and director of the Nanoelectronics Integrated Systems Center at NU. He was with IBM Microelectronics from 1997 to 1999. He has coauthored more than 130 technical papers and a book, and several book chapters. His primary research interests include digital integrated circuit design, interconnect, noise, innovative circuit simulation, and related circuit level issues in high performance VLSI circuits.

Dr. Ismail was selected as the 2002 IEEE circuits and systems society outstanding young author award winner, and received the National Science Foundation Career Award in 2002. He has been given the Best Teacher Award in the ECE Department, Northwestern University in 2002–2003. He is the chair elect of the CAS VLSI Technical Committee, an Editor-in-Chief of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, was on the editorial board of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: FUNDAMENTAL THEORY AND APPLICATIONS, and a guest editor for a special issue of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS on "On-Chip Inductance in High Speed Integrated Circuits". He has also chaired many conferences such as GLSVLSI, IWSOC, ISCAS.

Rajiv V. Joshi (F'02) received the B.Tech degree from Indian Institute of Technology, Bombay, India, M.S. degree from Massachusetts Institute of Technology, Cambridge, and the Doctorate degree in engineering science from Columbia University, New York, NY.

He is a research staff member with T. J. Watson Research Center, IBM, Yorktown, NY. From 1981 to 1983, he was with GTE Research Lab, Waltham, MA. He joined IBM in November 1983, and since then is working in VLSI design systems, science, and technology. He worked on 1.25 μm nMOS, and CMOS, sub-0.5 μm CMOS logic, DRAM and SRAM technologies. He developed novel interconnect processes and structures for Aluminum, tungsten and Copper technologies which are widely used in IBM for various sub-0.5 μm memory and logic technologies as well as across the globe. His circuit related work includes design of register files, registers, latches, L1 caches-directory, TLB, IO circuits development of physical design tools, and CAD-based library generation and circuit designs in SOI technology. He contributed to S/390 Alliance processor design, working in both circuit design and CAD tools. The Alliance G5 chip was a very successful IBM product and Joshi received IBM Research Division Awards for his contributions to it and each of the follow-on processor designs. He jointly published a paper with IBM Poughkeepsie team on 2 GHz SRAM in G6 processor, which received worldwide attention. He received an Outstanding technical achievement award for his contributions to G6. He contributed through IP and designs to IBM PowerPC program taking a leadership role in SRAM technology, cell analysis/modeling and stability enhancement. He successfully led the technology driven SRAM at IBM Server Group. He is a

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.

master inventor and key technical leader at IBM Research Division. He has authored and coauthored over 128 research papers and presented several invited and keynote talks. He holds 128 U.S. patents in addition to several pending patents.

Dr. Joshi was a recipient of 46 invention plateau achievement awards from IBM and won two divisional patent portfolio awards for cross-licensing and utilization of his patents in the IBM products, 5 Research Division Awards, several top 10% patent awards (for licensing activities), 3 Corporate Patent Portfolio Awards from IBM for licensing contributions (June 6, 2002 and May 26, 2004, May 15 2007), the Lewis Winner Award in 1992 for an outstanding paper he coauthored at the International Solid State Circuit Conference, and the "Distinguished Alumnus Award" in the year 2008 from IIT, Bombay. He was instrumental in starting interconnect workshop in early 1980's. He chaired advanced interconnect conferences sponsored by MRS and served as an editor of the proceedings. He is elected as an IEEE fellow for 2002 for contributions to chip metallurgy materials and processes, and high performance processor and circuit design. He is actively involved in IEEE ISLPED (International Symposium Low Power Electronic Design) IEEE VLSI design, IEEE International SOI conf (2000–2003), ISQED Program committees. He was a general chair for ISLPED Conference of 2004.

Jing-Yang Jou (F'05) received the B.S. degree in electrical engineering from National Taiwan University, Taiwan, R.O.C., and the M.S. and Ph.D. degrees in computer science from the University of Illinois at Urbana-Champaign, Urbana-Champaign, in 1979, 1983, and 1985, respectively.

He is currently the Vice Chancellor (Academic Affairs), University System of Taiwan (consisting of four research universities: National Central University, National Chiao Tung University, National Tsing Hua University, and National Yang Ming University). He is the Executive Director of National SoC Program since April 2007. He was the Director General of National Chip Implementation Center, National Applied Research Laboratories, Taiwan, from February 2004 to June 2007. He was a full Professor and was Chairman of Electronics Engineering Department from 2000 to 2003 with National Chiao Tung University, Hsinchu, Taiwan. Before joining Chiao Tung University, he was with GTE Laboratories from 1985 to 1986 and with AT&T Bell Laboratories, Murray Hill, NJ, from 1986 to 1994. His research interests include logic and physical synthesis, design verification, CAD for low power and Network on Chips. He has published more than 160 technical papers.

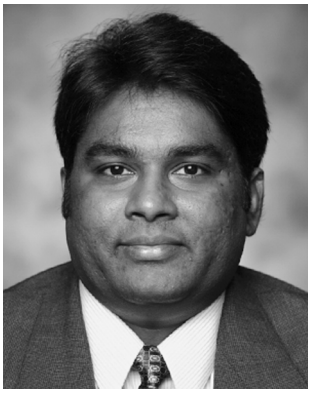
Dr. Jou was a recipient of the Distinguished Paper Award of the IEEE International Conference on Computer-Aided Design in 1990, the Outstanding Academy-Industry Cooperation Achievement Award granted by Ministry of Education (MOE), Taiwan, in 2002, and the Outstanding Electrical Engineering Professor Award from CIEE in 2006. He was elected to the President of the Taiwan Integrated Circuit Design Society (TICD) 2007–2008. He serves as Associate Editor for IEEE Transactions on Very Large Scale Integration Systems. He was the Technical Program Chairs of 2007 VLSI-DAT, the 12th VLSI Design/CAD Symposium (2001), and the Asia-Pacific Conference on Hardware Description Languages (APCHDL'97). He was the Conference Chair of 2008 VLSI-DAT, the Honorary Chair of International Workshop on Multi-Project Chip (IWMC'06, 2006), and the Executive Chair of the 2nd Taiwan-Japan Microelectronics International Symposium (2002).

Byunghoo Jung received the B.S. degree from Yonsei University, Korea, in 1990, the M.S. degree from KAIST, Korea, in 1992, and the Ph.D. degree from the University of Minnesota, Twin Cities, in 2005.

From 1992 to 1999, he was with Samsung Electronics, Korea, where he was involved in the design of video signal driver circuits for flat panel display. Following receipt of his Ph.D. in January 2005, he was with Qualcomm, San Diego, CA, as a Senior RF IC Designer until he joined the School of Electrical and Computer Engineering, Purdue University as an Assistant Professor in August 2005. His research interests include high-speed analog and RF circuit design for wireless communications, high speed I/Os, and bio-telemetry systems. He is the first place winner of the 2002–2003 SRC SiGe BiCMOS Design Challenge (as a lead designer) and the 2007–2008 SRC/SIA Design Challenge (as a lead faculty), and holds 10 U.S. patents.

Dr. Jung has been serving as a Cochair of the DAC/ISSCC Student Design Contest (SDC) since October 2006, and as a member of the Analog Signal Processing Technical Program Committee (ASPTPC) in the IEEE Circuits and Systems Society since May 2006.

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.



Srinivas Katkoori (SM'03) received the doctoral degree in computer engineering from the University of Cincinnati, Cincinnati, OH, in 1998.

In Fall of 1997, he joined the Department of Computer Science and Engineering, University of South Florida, Tampa, as an Assistant Professor. In 2004, he was tenured and promoted as an Associate Professor. His research interests include the general area of VLSI CAD algorithms and design methodologies. Specific research areas include high level synthesis, low power synthesis, FPGA synthesis, and radiation tolerant CAD for FPGAs. To date, he has published over 50 peer-reviewed journal and conference papers. He holds one U.S. Patent (6 963 217).

Dr. Katkoori was a recipient of the 2001 National Science Foundation (NSF) CAREER Award, the inaugural 2002-2003 University of South Florida Outstanding Faculty Research Achievement Award, and the 2005 Outstanding Engineering Educator Award from the IEEE Florida Council (Region 3). Besides NSF, his research sponsors include Honeywell, NASA JPL, and Florida I4 High Tech Corridor Initiative. He serves on technical committees of several VLSI conferences and as a peer reviewer for several VLSI journals. Since 1996, he has been serving as an Associate Editor of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He is a senior member of ACM.

Farinaz Koushanfar (S'99–M'06) received the Ph.D. degree in electrical engineering and computer science, the M.A. degree in statistics from the University of California, Berkeley, in 2005, the M.S. degree in electrical engineering and computer science from the University of California, Los Angeles (UCLA), in 2001, and the B.S. degree in electrical engineering from Sharif University of Technology, Tehran, Iran.

Since July 2006, she has been an Assistant Professor with the Electrical and Computer Engineering and Computer Science Departments, Rice University. She is also the Director of Texas Instruments (TI) DSP Leadership, Rice University. She was an open collaborative research fellow with Intel during the academic year 2003–2004. She held the Coordinated Science Lab (CSL) fellowship at the University of Illinois, Urbana-Champaign, during the academic year 2005–2006. Her research interests include the areas of VLSI security and protection, design methods for hardware security and trust, post-silicon IC characterization, sensor-based embedded systems, and low power.

Anshul Kumar received the B.Tech. and Ph.D. degrees from IIT Delhi, Delhi, India, in 1974 and 1980, respectively.

He is currently a Professor with the Department of Computer Science and Engineering, IIT Delhi. He has also served as the head of Department of Computer Science and Engineering as well as the Dean of Undergraduate Studies both at IIT Delhi. He has held visiting appointments at University of Southern California, Los Angeles, University of Edinburgh and Royal Institute of Technology, Stockholm. He has done extensive research and development in the area of hardware description languages and high level synthesis.

Dr. Kumar was a recipient of the President's Gold Medal for obtaining the first rank in all the disciplines of B.Tech. in 1974.

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.

Volkan Kursun received the B.S. degree in electrical and electronics engineering from the Middle East Technical University, Ankara, Turkey, in 1999, and the M.S. and Ph.D. degrees in Electrical and Computer Engineering from the University of Rochester, Rochester, NY, in 2001 and 2004, respectively.

He performed research on mixed-signal thermal inkjet integrated circuits with Xerox Corporation, Webster, NY, in 2000. During summers 2001 and 2002, he was with Intel Microprocessor Research Laboratories, Hillsboro, OR, responsible for the modeling and design of high frequency monolithic power supplies. During summer 2008, he was a visiting Professor with the Chuo University, Tokyo, Japan. He served as an Assistant Professor with the Department of Electrical and Computer Engineering, University of Wisconsin, Madison from August 2004 to August 2008. He has been an Assistant Professor with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, People's Republic of China, since August 2008. His current research interests include low voltage, low power, and high performance integrated circuit design, modeling of semiconductor devices, and emerging integrated circuit technologies. He is the author of the books, *Multi-Voltage CMOS Circuit Design* (Wiley, 2006) and *CMOS* (China Machine Press, 2008).

Dr. Kursun served on the editorial board of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: BRIEF PAPERS from 2005 to 2008. He is a member of the technical program and organizing committees of a number of IEEE and ACM conferences and serves on the editorial boards of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, and the *Journal of Circuits, Systems, and Computers* (JCSC). He has more than 80 publications and four issued and two pending patents in the areas of high performance integrated circuits and emerging semiconductor technologies.

Diana Marculescu (S'94–M'98) received the M.S. degree in computer science from University Politehnica of Bucharest, Romania, in 1991, and the Ph.D. degree in computer engineering from the University of Southern California, Los Angeles, in 1998.

She is currently an Associate Professor with the Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA. Her research interests include energy aware computing, CAD tools for low power systems, and emerging technologies (such as electronic textiles or ambient intelligent systems).

Dr. Marculescu was a recipient of a National Science Foundation Faculty Career Award (2000-2004), an ACM-SIGDA Technical Leadership Award (2003), the Carnegie Institute of Technology George Tallman Ladd Research Award (2004), and a Best Paper Award from IEEE Asia South-Pacific Design Automation Conference (ASPDAC 2005). She was an IEEE-Circuits and Systems Society Distinguished Lecturer (2004-2005) and is currently the Chair of the ACM Special Interest Group on Design Automation (SIGDA).

Malgorzata Marek-Sadowska received the M.S. degree in applied mathematics and the Ph.D. degree in electrical engineering from Politechnika Warszawska (Technical University of Warsaw), Warsaw, Poland.

From 1976 to 1982, she was an Assistant Professor with the Institute of Electron Technology, Technical University of Warsaw. She became a Research Engineer with the University of California at Berkeley, Electronics Research Laboratory, in 1982 and continued there until 1990, when she joined the Department of Electrical and Computer Engineering, University of California, Santa Barbara, as a Professor.

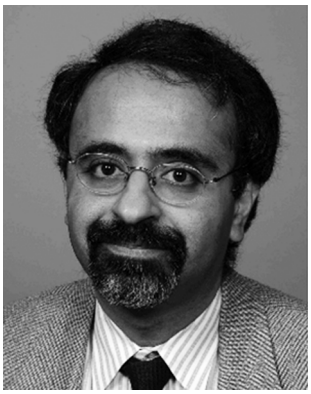
From 1993 to 1995, Dr. Marek-Sadowska was Editor-In-Chief of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS.

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.

Yehia Massoud (M'99) received the B.Sc. and M.Sc. degrees (with honors) from Cairo University, Cairo, Egypt, and the Ph.D. degree in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, in 1999.

In July 2003, he joined Rice University, Houston, TX, where he is the founding director of the Rice Automated Nanoscale Design Group (RAND) and an Associate Professor with the Electrical and Computer Engineering, Computer Science, and Applied Physics Departments. He was a member of the Technical Staff with the Advanced Technology Group, Synopsys Inc., Mountain View, CA, from 1999 to 2003. He is also the theme leader for Novel Interconnects and Architectures in the Southwest Academy of Nanoelectronics (SWAN), which is funded by the SRC Nanoelectronics Research Initiative. He leads research efforts targeting the modeling and design of innovative circuits, systems, and interconnect based on both carbon nanotubes and nanophotonic structures. He leads parallel research efforts targeting variability-aware optimization, modeling, and automated synthesis techniques for analog/RF/mixed signal circuits and systems as well as methodologies for interconnect-centric network-on-chip and thermally-aware design. He has published more than 150 papers in peer reviewed journal and conferences.

Dr. Massoud was a recipient of the Synopsys Special Recognition Engineering Award, the National Science Foundation CAREER Award for 2004, several Best Paper Award nominations, and the Best Paper Award at the 2007 IEEE International Symposium on Quality Electronic Design. He currently serves as the General Co-Chair of the 2009 ACM Great Lakes Symposium on VLSI (GLSVLSI). He is also an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS. He also serves on the Editorial board of the *Journal of Circuits, Systems, and Computers*. He has served as the Technical Program Cochair of the 2007 ACM Great Lakes Symposium on VLSI. He has chaired or cochaired conference tracks in several IEEE/ACM international conferences, such as the design automation track in ISCAS 2007, ISCAS 2008, ISCAS 2009, the VLSI Design track in GLSVLSI 2006, and the emerging technologies track in ISVLSI 2009. He has also served on the technical program committees of many of the key conferences in Electronic Design Automation, VLSI, and Nanotechnology, such as ICCAD, ISCAS, DATE, ISQED.



Kartikeya Mayaram (S'82–M'88–SM'99–F'05) received the B.E. (Hons.) degree in electrical engineering from the Birla Institute of Technology and Science, Pilani, India, in 1981, the M.S. degree in electrical engineering from the State University of New York, Stony Brook, in 1982, and the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1988.

He is currently a Professor with the School of Electrical Engineering and Computer Science, Oregon State University. From 1988 to 1992, he was a Member of Technical Staff in the Semiconductor Process and Design Center of Texas Instruments, Dallas. From 1992 to 1996, he was a Member of Technical Staff with Bell Labs, Allentown, PA. He was an Associate Professor with the School of Electrical Engineering and Computer Science, Washington State University, Pullman, from 1996 to 1999 and in the Electrical and Computer Engineering Department, Oregon State University, Corvallis, from 2000–2003. His research interests include the areas of circuit simulation, device simulation and modeling, simulation and modeling of substrate coupling in mixed-signal ICs, integrated simulation environments for microsystems, and analog/RF design.

Dr. Mayaram was a recipient of the National Science Foundation (NSF) CAREER Award in 1997. He has served on the technical program committees of several conferences and was on the editorial board of IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS as an Associate Editor from 1995 to 2001 and as the Editor-in-Chief from 2002 to 2005.

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.

Pramod Kumar Meher (SM'03) received the first class degrees of B.Sc. (Honors) and M.Sc. in physics and the Ph.D. degree in science from Sambalpur University, India, in 1976, 1978, and 1996, respectively.

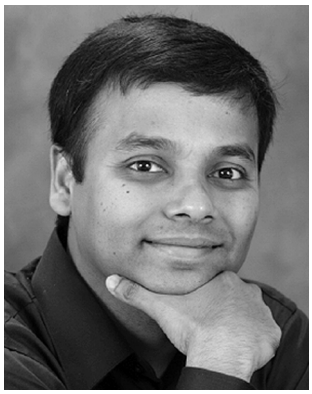
Currently, he is a Senior Scientist in the Institute for Infocomm Research, Singapore. Prior to this assignment, he was a visiting Senior Fellow with the School of Computer Engineering, Nanyang Technological University, Singapore, and has served as a Professor with Utkal University, Bhubaneswar, India, between 1997 and 2002. He has worked extensively on algorithm-architecture codesign for VLSI signal processing, and has published several papers on ASIC and FPGA implementation of orthogonal transforms, digital filters and arithmetic units. His current research interests include the design and optimization of dedicated and reconfigurable architectures for computation-intensive problems in signal processing, image processing, secure communication and bioinformatics for resource-constrained applications.

Dr. Meher was a recipient of the Samanta Chandrasekhar Award for excellence in research in Engineering and Technology for the year 1999. He is a Chartered Engineer of the Engineering Council of United Kingdom, a Fellow of The Institution of Electronics and Telecommunication Engineers (IETE) of India, and a Fellow of the Institution of Engineering and Technology (IET). Currently, he is also serving as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS and the *Journal of Circuits and Systems for Signal Processing*.

Seda Ogrenci Memik (M'98–SM'05) received the B.S. degree in electrical and electronic engineering from Bogazici University, Istanbul, Turkey, and the Ph.D. in computer science from University of California, Los Angeles.

She is currently an Assistant Professor with the Electrical Engineering and Computer Science Department, Northwestern University, Evanston, IL. Her research interests include embedded and reconfigurable computing, thermal-aware design automation, and thermal management for high performance microprocessor systems.

Dr. Memik was a recipient of the National Science Foundation Early Career Development (CAREER) Award in 2006. She has served as technical program committee member, organizing committee member, sub-committee and track cochair of several conferences, including ICCAD, DATE, FPL, and GLSVLSI and she is currently serving on the Editorial Board of IEEE Transactions on VLSI.



Subhasish Mitra is an Assistant Professor with the Departments of Electrical Engineering and Computer Science, Stanford University, Stanford, CA, where he leads the Stanford Robust Systems Group. His research interests include robust system design, VLSI design, CAD, test, and validation, and Design for emerging nanotechnologies. Prior to joining Stanford, he was a Principal Engineer with Intel Corporation.

He has coauthored over 100 technical papers and has invented design and test techniques that have seen widespread proliferation in the semiconductor industry. His X-Compact technique for test compression is used by over 50 Intel products, and is supported by major CAD tools. His work on imperfection-immune circuits using carbon nanotubes, jointly with his students and collaborators, has been highlighted as "a significant breakthrough" by the Semiconductor Research Corporation, MIT Technology Review, and EE Times.

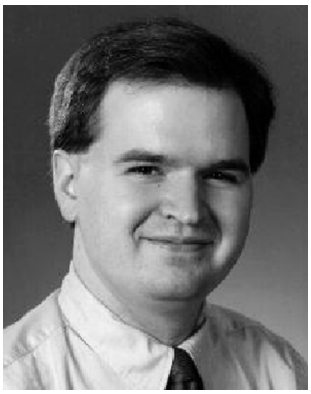
Prof. Mitra was a recipient of the Presidential Early Career Award for Scientists and Engineers (PECASE, the highest honor bestowed by the US government on early career outstanding scientists and engineers), the National Science Foundation CAREER Award, the Terman Fellowship, the IEEE Circuits and Systems Society Donald O. Pederson Award for the Best Paper published in the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, the ACM SIGDA Outstanding New Faculty Award, the IEEE/ACM Design Automation Conference Best Paper Award, a Divisional Recognition Award from Intel "for a Breakthrough Soft Error Protection Technology," Intel Design and Test Technology Conference Best Paper Award for his work on built-in soft error resilience, and the Intel Achievement Award, Intel's highest corporate honor, "for the development and deployment of a breakthrough test compression technology."

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.

Kartik Mohanram (S'00–M'04) received the B.Tech. degree in electrical engineering from IIT, Bombay, in 1998, and the M.S. and Ph.D. degrees in computer engineering from the University of Texas at Austin, Austin, in 2000 and 2003, respectively.

He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Rice University, Houston, TX. His primary research interests include computer engineering and systems, with an emphasis on modeling, simulation, and computer-aided design for scaled electronic technologies.

Dr. Mohanram was a recipient of the NSF CAREER Award, the ACM/SIGDA Technical Leadership Award, and the A. Richard Newton Graduate Scholarship.



Chris Myers received the B.S. degree in electrical engineering and Chinese history from the California Institute of Technology, Pasadena, CA, in 1991, and the M.S.E.E. and Ph.D. degrees from Stanford University, Stanford, CA, in 1993 and 1995, respectively.

He is a Professor with the Department of Electrical and Computer Engineering, University of Utah, Salt Lake City. He is the author of over 80 technical papers and the textbook *Asynchronous Circuit Design* (Kluwer, 1990). He is also a coinventor on four patents. His research interests include algorithms for the analysis of real-time concurrent systems, analog error control decoders, formal verification, asynchronous circuit design, and the modeling and analysis of genetic regulatory circuits.

Dr. Myers was a recipient of an NSF Fellowship in 1991, an NSF CAREER Award in 1996, and Best Paper Awards at Async1999 and Async2007.

Sule Ozev received the B.S. degree in electrical engineering and the M.S. and Ph.D. degrees in computer science and engineering from Bogazici University, Turkey, in 1995, 1998, and 2002, respectively.

Between 2002 and 2008, she was an Assistant Professor with the Electrical and Computer Engineering Department, Duke University. In 2008, she joined the Electrical Engineering Department, Arizona State University, Tempe, where she currently holds an Associate Professor position. Her research interests include system and circuit level test approaches for analog/RF circuits, hierarchical fault modeling, simulation, test evaluation, and process variability analysis for mixed-signal circuits.

David Z. Pan (S'97–M'00–SM'06) received the Ph.D. degree in computer science from the University of California, Los Angeles, in 2000.

From 2000 to 2003, he was a Research Staff Member with the IBM T. J. Watson Research Center, Yorktown Heights, NY. He is currently an Associate Professor with the Department of Electrical and Computer Engineering, the University of Texas, Austin. He has published over 100 technical papers and is the holder of six U.S. patents. His research interests include nanometer physical design, design for manufacturing, low-power vertical integration design and technology, and CAD for emerging technologies.

Dr. Pan was a recipient of a number of awards for his research contributions and professional services, including the ACM/SIGDA Outstanding New Faculty Award (2005), NSF CAREER Award (2007), SRC Inventor Recognition Award (2000 and 2008), IBM Faculty Award (2004-2006), IBM Research Bravo Award (2003), SRC Techcon Best Paper in Session Award (1998 and 2007), Dimitris Chorafas Foundation Research Award (2000), ISPD Routing Contest Awards (2007), eASIC

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.

Placement Contest Grand Prize (2009), several Best Paper Award Nominations at DAC/ICCAD/ASPDAC, and ACM Recognition of Service Award (2007 and 2008). He is a Cadence Distinguished Speaker in 2007 and an IEEE CAS Society Distinguished Lecturer for 2008–2009. He is a member of the ACM/SIGDA Technical Committee on Physical Design and a member of the Technical Advisory Board of Pyxis Technology Inc. He is in the Design Technology Working Group of International Technology Roadmap for Semiconductor. He has served in the Technical Program Committees of major VLSI/CAD conferences, including ASPDAC (Topic Chair), DAC, DATE, ICCAD, ISPD (Program Chair), ISQED (Topic Chair), ISCAS (CAD Track Chair), SLIP, GLSVLSI, ACISC (Program Co-chair), ICICDT, and VLSI-DAT. He is the General Chair of ISPD 2008 and Steering Committee Chair of ISPD 2009. He is an officer in the IEEE CANDE Committee (Workshop Chair in 2007 and Secretary in 2008). He has served as an Associate Editor for IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS (TCAD), IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: BRIEF PAPERS, and *IEEE CAS Society Newsletter*. He is also a Guest Editor of TCAD Special Section on "International Symposium on Physical Design" in 2007 and 2008.

Zebo Peng (M'91–SM'02) received the B.Sc. degree in computer engineering from the South China Institute of Technology, China, in 1982, and the Licentiate of Engineering and Ph.D. degrees in computer science from Linköping University, Linköping, Sweden, in 1985 and 1987, respectively.

He is currently a Full Professor of Computer Systems, Director of the Embedded Systems Laboratory, and Chairman of the Division for Software and Systems in the Department of Computer Science, Linköping University. He served as the Director of the National Graduate School of Computer Science in Sweden from 2006 to 2008. His current research interests include design and test of embedded systems, electronic design automation, SoC testing, design for testability, hardware/software codesign, and real-time systems. He has published more than 250 technical papers, and coauthored four books: *System Synthesis with VHDL* (Kluwer, 1997), *Analysis and Synthesis of Distributed Real-Time Embedded Systems* (Kluwer, 2004), *System-level Test and Validation of Hardware/Software Systems* (Springer, 2005), and *Real-Time Applications with Stochastic Task Execution Times* (Springer, 2007).

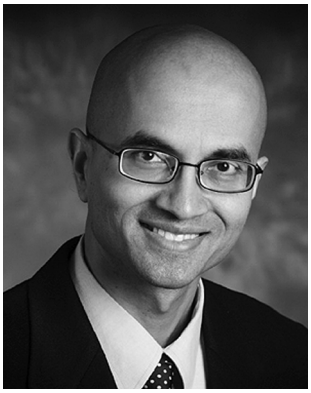
Prof. Peng was a recipient of two Best Paper Awards at the European Design Automation Conferences (1992 and 1994), a Best Paper Award at the IEEE Asian Test Symposium (2002), a Best Paper Award at the Design Automation and Test in Europe Conference (2005), and a Best Presentation Award at the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (2003). He serves currently as an Associate Editor of the IEEE TRANSACTION ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, the *VLSI Design Journal*, and the *EURASIP Journal on Embedded Systems*. He has served as the Guest Editor for the Special Issue on "Emerging Strategies for Resource-Constrained Testing of System Chips" in the IEE Proceedings for Computer and Digital Techniques and the special issue on "Design Methodologies and Tools for Real-Time Embedded Systems" in the *Journal on Design Automation for Embedded Systems*. He has served on the program committee of a dozen international conferences and workshops, including ATS, ASP-DAC, DATE, DDECS, DFT, ETS, ITSW, MEMOCDE, and VLSI-SOC. He was the General Chair of the 6th IEEE European Test Workshop (ETW 01) and the Program Chair of the 7th IEEE Design & Diagnostics of Electronic Circuits & Systems Workshop (DDECS 04), the 12th IEEE European Test Symposium (ETS 07), and the 11th Design Automation and Test in Europe Conference (DATE 08). He is currently the Chair of the IEEE European Test Technology Technical Council (ETTTC), and has been a Golden Core Member of the IEEE Computer Society since 2005.

Srivaths Ravi (SM'05) received the B.Tech degree in electrical and electronics engineering and the Siemens Medal from the Indian Institute of Technology, Madras, India, and the M.A. and Ph.D. degrees in electrical engineering from Princeton University, Princeton, NJ.

He is a Member of the Group Technical Staff with the DSP Systems Group, Texas Instruments, India, where he is responsible for DFT implementation in TI's multimedia chips and also for furthering various test methodology initiatives in power-aware test, scan compression, and ATPG. Prior to TI, he was a research staff member with NEC Laboratories America, Princeton, NJ, where he was mainly responsible for R&D projects in embedded security and low power design. His work at NEC has contributed to the design of the mobile security processor MOSES used in NEC's cellphone chips, as well as to the development of RTL and C-based power estimation capabilities in NEC's Cyber design framework. His contributions have resulted in 8 filed patents (4 issued). While at NEC, he also held a visiting research collaborator position with the Department of Electrical Engineering, Princeton University. He has several publications in these areas.

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.

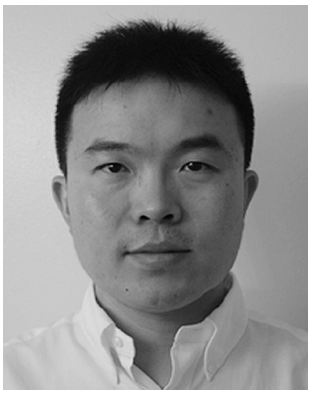
Dr. Ravi was a recipient of four Best Paper Awards and NEC Laboratories's Technology Commercialization Award. He serves in the organizing and technical program committees of various leading conferences.



Naresh R. Shanbhag (F'06) received the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, in 1993.

Since August 1995, he has been with the Department of Electrical and Computer Engineering, and the Coordinated Science Laboratory, where he is currently a Professor. From 1993 to 1995, he worked at AT&T Bell Laboratories, Murray Hill, NJ, where he was the lead chip architect for AT&T's 51.84 Mb/s transceiver chips over twisted-pair wiring for Asynchronous Transfer Mode (ATM)-LAN and very high-speed digital subscriber line (VDSL) chip-sets. In 2000, Dr. Shanbhag cofounded and served as the Chief Technology Officer of Intersymbol Communications, Inc., a venture-funded fabless semiconductor startup that provides mixed-signal ICs for electronic dispersion compensation of OC-192 optical links. In 2007, Intersymbol Communications, Inc., was acquired by Finisar Corporation, Inc., where he is presently serving as a Senior Scientist on a part-time basis. His research interests include the design of integrated circuits and systems for broadband communications including lowpower/high-performance VLSI architectures for error-control coding, equalization, as well as integrated circuit design. He has numerous publications in this area and holds four U.S. patents. He is also a coauthor of the research monograph *Pipelined Adaptive Digital Filters* (Kluwer, 1994).

Dr. Shanbhag was a recipient of the 2006 IEEE JOURNAL OF SOLID- STATE CIRCUITS Best Paper Award, the 2001 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS Best Paper Award, the 1999 IEEE Leon K. Kirchmayer Best Paper Award, the 1999 Xerox Faculty Award, the Distinguished Lecturership from the IEEE Circuits and Systems Society in 1997, the National Science Foundation CAREER Award in 1996, and the 1994 Darlington Best Paper Award from the IEEE Circuits and Systems Society. He served as an Associate Editor for the IEEE TRANSACTION ON CIRCUITS AND SYSTEMS—II: BRIEF PAPERS (1997–1999) and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (1999–2002), respectively. He is currently serving on the technical program committees of major international conferences such as the International Solid-State Circuits Conference (ISSCC), the International Conference on Computer-Aided Design (ICCAD), the International Symposium on Low- Power Design (ISLPED), the International Conference on Acoustics, Speech and Signal Processing (ICASSP), and others.



Li Shang received the Ph.D. degree from Princeton University, Princeton, NJ, and the B.E. degree with honors from Tsinghua University, Beijing, China.

He is an Assistant Professor with the Department of Electrical and Computer Engineering, University of Colorado, Boulder. He has published in the areas of design automation for embedded systems, design for nanotechnologies, distributed computing, and computer architecture.

Dr. Shang's recent work has been nominated for the Best Paper Award at ICCAD 2008, DAC 2007, and ASP-DAC 2006. His work on temperature-aware on-chip network has been selected for publication in MICRO Top Picks 2006. He was a recipient of the Best Paper Award at PDCS 2002 and of his department's teaching award in 2006.

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.

Ankur Srivastava received the B.S. degree in technology from the Indian Institute of Technology, Delhi, India, in 1998 with electrical engineering major, the M.S. degree in computer engineering from the Department of Electrical and Computer Engineering (ECE), Northwestern University, Evanston, IL, in 2000, and the Ph.D. degree from the Computer Science Department, University of California Los Angeles, Los Angeles (UCLA), in 2002.

He is an Assistant Professor with the Electrical and Computer Engineering Department, the University of Maryland, College Park, and also with a joint appointment with the Institute for Systems Research. He has been working at the University of Maryland since October 2002. His main area of interest is VLSI CAD for high performance and low power VLSI circuits.

Dr. Srivastava was a recipient of the "Outstanding Ph.D. Award" from the Computer Science Department, UCLA and the George Corcoran Memorial Outstanding Teaching Award by the ECE Department of University of Maryland.

Susmita Sur-Kolay (SM'05) is currently an Associate Professor with the Advanced Computing and Microelectronics Unit of the Indian Statistical Institute, Kolkata, India. From 1993 to 1999, she was a Reader with the Department of Computer Science and Engineering, Jadavpur University, Kolkata, India. In 1992, she visited the University of Nebraska, Lincoln, and in 2002, she was a Visiting Faculty with the Academic Research Program of Intel Corporation, USA. Her research contributions have been in the area of algorithmic CAD for VLSI physical design, fault modeling and testing, synthesis of quantum computers, graph and geometric algorithms. She has been collaborating with researchers both in academia and industry in India, USA, France, Japan, and has been the Principal Investigator of research projects funded by industry and government agencies. She has authored several technical papers in international journals and refereed conference proceedings.

Dr. Sur-Kolay was a recipient of President of India Gold Medal (summa cum laude) at IIT Kharagpur in 1980. She has served on the Program Committees of many International Conferences and was the Technical Program Chair of the 18th International Conference on VLSI Design, 2005. She has also been reviewer for many international journals and is presently on the editorial board of Proceedings of IEE CDT. She is a Member of IEE and VLSI Society of India.

Zhongfeng Wang received the B.E. and M.S. degrees from the Department of Automation, Tsinghua University, Beijing, China, and the Ph.D. degree from the Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, in 2000.

From 1990 to 1995, he worked for Beijing Huahai New Technology Development Co., Beijing, China, as a Principal Engineer and Technical Manager. He joined Morphics Technology Inc. (now part of Infineon Technology) in 2000 as a member of the Technical Staff. In 2002, he moved to National Semiconductor Co. as a Senior Staff Design Engineer. In 2003, he became an Assistant Professor with the School of Electrical Engineering and Computer Science (EECS), Oregon State University, Corvallis. Since June 2007, he has been a Senior Principle Scientist with Broadcom Corporation, Irvine, CA. His current research interests include the area of low power/high speed VLSI design, specifically VLSI Design for digital signal processing, digital communications (including error correction codes), and cryptography systems.

Dr. Wang was the recipient of the Best Student Paper Award at the 1999 IEEE Workshop on Signal Processing Systems (SiPS '99) and corecipient of the IEEE Circuits and Systems (CAS) Society VLSI Transactions Best Paper Award in 2007. He has published over 70 technical papers and has filed numerous U.S. patent applications. He served as an Associate Editor (AE) for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS from 2003 to 2005 and is serving as Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: BRIEF PAPERS. He has also served as technical program committee member for several IEEE and ACM conferences. He is currently in the technical committee of VLSI Systems and Applications (VTA-TC) and in the technical committee of Circuits and Systems for Communications (CASCOM) in the IEEE CAS Society. He is a member of Sigma Xi Society and a senior member of the IEEE Circuits and Systems Society.

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.

Stacey Weber Jackson received the B.A. degree in sociology and the M.S.W. degree in social work from Rutgers University, New Brunswick, NJ, in 1998 and 2002, respectively.

She is a New Jersey state certified social worker. She is currently serving as the Editorial Assistant for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.

Yuan Xie received the B.S. degree in electronic engineering from Tsinghua University, Beijing, China, and the M.S. and the Ph.D. degrees in electrical engineering from Princeton University, Princeton, NJ.

He is an Associate Professor with the Computer Science and Engineering Department, Pennsylvania State University (Penn State), University Park. Before joining Penn State in Fall 2003, he was with IBM Microelectronic Division's Worldwide Design Center at Essex Junction, VT. He has published more than 100 conference and journal papers, on topics including VLSI design, computer architecture, design automation, and embedded system designs.

Dr. Xie was a recipient of the SRC Inventor Recognition Award in 2002, NSF CAREER Award in 2006, IBM Faculty Award in 2008, the Best Paper Award in ASP-DAC 2008 and ASICON 2001, and Best Paper Award Nomination in ICCAD 2006 and ASP-DAC 2009.

Authorized licensed use limited to: IEEE Xplore. Downloaded on April 12, 2009 at 21:47 from IEEE Xplore. Restrictions apply.